Fault locator for distribution systems, utilising fault arc noise

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Fault Locator For Distribution Systems, Utilising Fault Arc Noise

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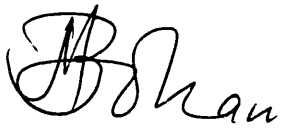

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DEDICATED TO MY PARENTS WITH LOVE AND RESPECTS

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SUMMARY

This thesis is concerned with design developments of a commercially failed fault locator. Details of design modifications and simulation test procedures of the design developments of the fault locator are described in this thesis. The simulation tests are necessary to ensure success of the new design before going into production. This developed fault locator can be universal as it requires no extra power source to operate, no amplification of its output signal, and no equipment or link for communicating the output signal to operate local or remote indicating and recording equipments. It diagnoses 11kV line system fault simply from fault noise frequencies. The distribution conductors themselves act as communication link. Output signal obtained from the fault locator at any place along the distribution conductors is high enough to operate conventional alarms and relays. Although this fault locator is designed and tested on simulation software (EMTP) for 11 kV distribution system, it can easily be adopted for voltages higher than 11kV. With modification in the method of its application, this fault locator locates virtually all earth faults on the distribution system. Due to high, reliable and quick responding output, its output can also best be used for protection of lines and equipments.

Principle of the fault locator is based on coordination of two types of analogue filters. The first filter (called trap circuit) blocks a band of frequencies while the second filter (called stack tuner) detects existence of the same band of frequencies. Depending upon the method of its application, if any of the stack tuners detects the signal (i.e. it gives an output signal to operate an alarm etc), a fault is located.

Test results (confirming satisfactory performance) of the fault locator are obtained from fault simulations, under conditions similar to real supply of power to three phase loads, line tappings and operation of circuit breaker to separate faulty section. Capacitor banks which are often used to improve voltage regulation and power factor are also included in the simulation network. The faults, for which the fault locator is tested by simulation, include solid earth fault, fault through 1000 ohms resistance, earth arcing fault, open phase fault and lightning strokes. The fault locator in each case detects the fault in its exact place of occurrence.

TABLE OF CONTENTS

Symbols

L, L_{stack}	Stack tuner inductance, H
R_0, R_{stack}	Stack tuner resistance equivalent to surge impedance, Ω
EMF	Electro motive force of distribution system source, V
f_0	Resonent frequency of a fault locator, its trap and stack filters, Hz
MVA	Total 3-phsae rating capacity of voltage source or load, Mega Volt-amperers
VA_{ph}	Terminal load rating per phase
Z_{ph}	Per phase terminal load impedance, Ω
NA,NB, NC	Node names on each phase at terminal N*
LMA6,LMB6 LMC6	Node names on phase A,B & C at terminal LM*6
FA4,FB4,FC4	Node names on phase A,B & C at lerminal F*4
Z_{L1}	Per phase impedance at each of nodes NA, NB & NC, Ω
Z_{L2}	Per phase impedance at each of nodes LMA6, LMB6 & LMC6, Ω
Z_{L3}	Per phase impedance at each of nodes FA4, FB4 and fc4, Ω
L_1, L_2, L_3	Per phase loads inductance at nodes N*, LM*6 and F*4 respectively, H
C_1, C_2, C_3	Per phase capacitance of capacitor banks at nodes N*, LM*6 & F*4 respectively, F
EMTP	Eletro magnetic transient program (name of a software to determine transients in electrical systems)
MVA_{sec}	Total capacity of the 3-phase voltage source for 3-phase distribution system
δT	Incrimental time, seconds
C_t	Total capacitance of capacitor banks per phase, F
R_0	Surge imedance of the distribution lines, Ω
Z_U, Z_M, Z_L	Impedace of upper, middle and lower branches of a 3-branch single or twin trap, Ω
Z_{UM}	Combined impedance of upper and middle branches of a trap circiut, Ω
Z_{trap}	Total impedance of a trap circuit, Ω
f_h	High resonent frequency of 1st trap of twin trap, Hz

f_L	Low resonent frequency of 2nd trap of twin trap, Hz
SEP	Seperation between f_h and f_L, Hz
C_L	Capacitance of low frequency trap, F
C_h	Capacitannce of high frequency trap, F
R_n	Resistance of inductive branch of the parallel resonant circuit of stack tuner, Ω
L_n	Inductane of inductive branch of parallel resonent circuit of stack tuner, H
C_n	Capacitance of capacitive branch of parallel resonant circuit of stack tuner, F
Z50	Impedance of stack tuner at 50 Hz, H
BW, B	Band width of a resonant circuit or filter, Hz
BW_{st}	Bandwidth of stack tuner, Hz
p.f.	power factor of a circuit or load
X_l	Inductive reactance, Ω
X_c	Capacitive reactance, Ω
(X_l-X_c)	Total reactance of series inductive reactance X_l and capacitive reactance X_c, Ω
v_i	Input voltage to a filter or circuit, V
V_o	Output voltage across a branch or filter output terminals, V
$Z_{parallel}$, Z,	Impedance of parallel resonant circuit, Ω
Z_s	Impedance of a series branch, Ω
R_1, R_2	Resistance of each power coil in twin trap circuit, Ω
L_1, L_2	Inductance of each power coil in twin trap ciruit, H
L_{effect}	Effective inductance of a trap circuit, H
L_{small}	Small value of inductance used in parallel branch of stack tuner, H
v_{arc}, i_{arc}	Voltage and current of arcing V, A
R_{arc}	Resistance of arcing fault, Ω
I_p	Maximum peak value of current from steady state fault simulation test, A
i_a	Actual instantaneous arc current, A
R_p	Instantaneous arc resistance, Ω
R_{rise}, R_{fall}	Arc resistances during rise and fall of arcing fault current near zero, Ω
RB	Average resistance of R_{rise} and R_{fall}, Ω

Chapter-1

INTRODUCTION

1.1 Purpose of research

The sole purpose of this research is to develop a fault locator which can locate almost all types of faults immediately after their occurrence in a power system with high accuracy so that long hours of power outage , loss of life, damage to equipment and property , stoppage of industry and decline of economy resulting from long hours of power failure can be avoided or minimised. By efficient fault location, power becomes cheap, safe, efficient, neat, clean and reliable. For this purpose the fault-locator, on which considerable work is already done [1-9], is selected as a basis for further developments. The previous research [1-9] was in fact an attempt to improve performance of a commercially available fault locator, which in its present manufactured form is unable of proper performance. Design and performance of this previously published and commercially available fault locator is investigated, tested, analysed, redesigned and retested [10-11] for improvements and better performance in a real 3-phase network system supplying some balanced 3-phase loads. Success of this research will finally be used to modify parameters of the commercially available fault locator so that it can localise high resistance faults as well as low level arc faults and discharges in 11 kV distribution systems.

Reasons for the unsatisfactory results of the previous fault locators are (i) use of series LCR circuit and (ii) poor design of the LCR circuit. As analysed in section 3.3 on page 16, the previous fault locator quoted in references [1-3], gave bandwidth of 636 Hz of the trap circuit against wide bandwidth of 31250 Hz of its stack tuner. For successful operation of the fault locator, bandwidth of its stack tuner should be less than bandwidth of the corresponding trap circuit. As this condition was absent in the previous fault locator, it failed in proper operation.

The second major reason of failure of the previous fault locator is use of series LCR stack tuner in itself. Investigations on series LCR

stack tuners in chapter 7 proves that the LCR stack tuner is not capable of filtering signals properly. For this reason new improved stack tuner, known as series/parallel stack tuner, is designed to replace the old series LCR stack tuner. The new series/parallel stack tuner replaces constant value of surge impedance resistance R_0 of the series LCR stack tuner by an equivalent dynamic resistance at resonant frequency. This change enables the new series/parallel stack tuner to have virtually zero resistance at off the resonant frequencies and consequently zero output at off the resonant frequencies contrary to the old series LCR stack tuner. Full justification of this principle is provided in chapter 7 on page 57, 61 and 64.

Now further developments are carried out and the computer investigations of the latest design of the fault locator show much better performance for reliable signal, low cost, fast response etc. The computer tests proved that this fault locator is successful in fault location.

1.2 The fault as a source of frequency generation

We know from our every day experience that faults create transients, harmonics, noises and surges which are made from a combination of sinusoidal wave forms of different frequencies, ranging from dc to Mega Hertz [1-13]. Formation of these transient wave forms from high frequency components can be proved by Fourier Analysis [14,15] or experimentally in a laboratory by combining sinusoidal waveforms of different frequencies and amplitudes. As the shape of a fault transient voltage or current depends upon (i) type of fault, (ii) fundamental frequency of power supply, (iii) instantaneous value of voltage and current of the power frequency, (iv) magnitude and type of circuit parameters, etc, amplitude of each component frequency of the fault transient is different for different transient [12-15]. These components or noise frequencies, are created in all non-arc as well as arc type faults. The difference between the two types of faults is that in non-arc type fault, frequencies die rapidly as the fault current settles down to steady state fault value in a short time, whereas in arc type fault, high frequencies are repeated continuously but non-periodically till the fault is cleared. Thus non-arc or non-spark type faults are relatively difficult, compared to arc type

faults, to localise by conventional frequency type locators.

The noise frequencies generated by a fault, in a power system, have been very widely used in fault detection by radio frequency pick up coils and other systems. Faults through constant resistance, short circuit, open circuit etc also produce wideband fault noise frequencies, but the fault localisation is possible only in cases where noise frequencies are immediately recorded and that the records produced from different locations produce different and distinct magnitude of noises.

1.3 Literature survey of work related to the new fault locator

Working principle of new fault locator presented in this thesis is based upon fault generated transient frequencies. The travelling wave methods of fault location have been used in underground cables and proposed for overhead lines systems since 1931 [16-31]. At present there is no viable method in practice for fault localisation for over head distribution system. Arcing as well as non-arcing faults can be detected by fault generated transient frequencies. The earlier researchers [1-4], although did not present a perfect answer to fault location, they succeeded to devise fault protection equipments and they are also pioneers of this work on fault localisation using fault generated noise. To detect the presence of a narrow band of transient frequencies resulting from a fault at any particular point along power lines, filters are inserted at suitable places in a travelling wave algorithm. Graham, Carlson and Granberg [19] monitored distribution feeder input impedance at high frequencies in the range of 50 kHz to 100kHz. Balser [20] used 3rd and 5th harmonic frequencies to identify high impedance arcing faults. Aucoin and Russell [13] examined high impedance fault protection in the range of 2 kHz to 10 kHz. Aucoin and Russell, in an other paper [21], used burst noise signals during arcing and was able to use frequencies near, below and above 60 Hz. EPRI [22] designed a fault detector at Texas A & M University to detect ground faults between 2 kHz and 10 kHz frequency components. Russell, Mehta and Chinchali [23] used low frequency components, particularly 180 Hz and 210 Hz, to detect presence of faults. Vilchech and Gonzalez [24] measured harmonic components of arcing faults and circuit breaker arcs. They concluded that arcs are mostly made of odd

harmonics and harmonic level mostly depends upon the impedance between source and arc points. Russell and Chinchali [25] described application of signal processing hardware and software using frequencies between 30 Hz and 360 Hz from arc faults. Clark and Horn [26] invented a low cost electronic circuitry sensor to detect directional faults. These and other [1-31] researchers show that fault noise frequencies have been used to detect fault and protect power system.

A.T.Johns and M. El-Hami [1-4] devised microprocessor application using digital filters in the detection of fault by unidirectional scheme and travelling wave algorithm. They used high frequency components for the detection of the fault. Early computer trials to locate faults proved successful and inspiring for further investigation to produce reliable higher output magnitude and better procedure for fault location.

Recent work carried by Burdi, El-Kateb and Johns [10-11], succeeded in obtaining high voltage fault signal output of 8 volts at 10 kHz and surrounding frequencies from direct phase measurement of 11kV power line. This is achieved by using newly designed fault locator. Old level of voltage detection was reported to be 250 mV. This low voltage was through 3-phase modal (1,-2,1) combination. Significance of difference in signal level achieved by Burdi and others becomes more apparent when quality of output signal and method of filtration are considered. This study uses single analogue filter compared to 6 separate filters used by El-Hami [1-4]. The 6 filters used by El-Hami are (i) 3 stack tuner filters in modal (1,-2,1) form , (ii) 1 digital filter, and (iii) 2 aliasing filters. The third significant difference between signal outputs of the two types of fault locators is that the signal achieved by this study is continuous in time after occurrence of a fault whereas signal in previous case is just a series of bursts. As this method does not require external or extra filtration or microprocessor, nevertheless, it has high output signal, it proves that this latest fault locator is cheaper, faster and more reliable than previous ones.

In this thesis, the fault locator is tested for fault conditions of unloaded and loaded distribution lines, line tappings, arc faults, circuit breaker operation, lightning strokes etc (not done before in a similar case). This study shows that the computer results are encouraging.

1.4 Need for an improved fault locator

Todays human civilization is totally dependent on electricity. Delay caused by inability to locate fault and restore electricity in power distributing systems merely for a quarter of an hour causes loss of millions of pounds in stoppage of work in industry, death and suffering to human beings and animals, damage to refrigerated food, fall in agricultural produce, and looting of goods of millions of pounds worth from shops during dark night in the darkness caused after the power outage etc. Long hours of delay in fault location (specially when the faults are frequent) and late restoration of electricity causes unrecoverable losses for years to electrical industry and government by fall in revenue and economy of the country. Average power restoration time, as reported by Clark and Horn [26], is two to four hours for developed countries like the U.K. and four to twenty four hours for developing countries like Pakistan [32-33]. Studies by Redmon, Chen and others, quoted in ref. [26] also show that substantial savings can be achieved in power systems in developed countries by spending money on improvement on fault monitoring and controlling. A fault can be repaired quickly, if and only if the fault is accurately and quickly located. As available methods of fault location are neither adequate nor efficient, there is a need for an improved fault locator.

1.5 Summary of the thesis & arrangement of chapters

This thesis is written in pleasant, natural, simple and systematic but brief form. In the initial chapter 1, introduction and background of the fault locator are given. In chapter 2 description of a practical network, its steady-state and transient behaviour are explained when supplying loads. To make the study, more comprehensive, shunt capacitor banks are introduced at appropriate places in the 3-phase network. Furthermore network description for installation of fault locators in the distribution system and general working principle of the fault locators are explained in chapter 3.

In chapters 4 and 5, design details of the fault locator (the trap and the stack tuner) are explained. Chapter 6 describes steady-state,

frequency-response characteristic of the designed fault locator. On comparison of results with that of previous fault locator [1-4], even the steady-state performance clearly shows that the new fault locator is superior in providing better results.

The transient performance of the fault locator is described in chapters 7 and onwards. In chapter 7, parameter related behaviour of the fault locator is computed for different parameters of the stack tuner. In chapter 8, effect of the shunt capacitor banks is studied and remedial measures are taken to save and safeguard performance of the fault locator from bad effect of capacitor banks. The fault locator performance under solid earth fault is studied in detail in chapter 9, where alternative arrangements of application of the fault locator are studied to understand proper application. Performance of the fault locator under (i) earth arcing fault, (ii) circuit breaker arc and (iii) lightning strokes are investigated in chapters 10, 11, and 12 respectively. Surge arrester effect is studied in chapter 12. Chapter 13 carries investigation into the performance of the fault locator for variation of stack tuner capacitance C_{stack}. This computer test gives important conclusion of the results when value of C_{stack} changes due to atmospheric changes, such as rain, heat, snow etc. Chapter 14 is for further investigations into transient behaviour of the fault locator for higher resonant frequency f_0 than 10 kHz for a solid earth fault. The final chapter 15 is summary of discussions, results and conclusions.

Chapter - 2

THE SELECTION OF THE DISTRIBUTION SYSTEM AND THE STUDY OF ITS BASIC CHARACTERISTICS BY EMTP

2.1 Single line diagram of a distribution network selected for simulation of faults

Figure 2.1 shows a complete single line diagram of a 3-phase 11 kV distribution network selected for installation of capacitors for p.f. improvement and fault locators. The complete network is made up of 13 sections of equal lengths (1.5 km), making total length of the network of 19.5 km. The first 9 sections, from JD*F to F*3, and F*2 to N* are made from stranded aluminum conductor with total nominal diameter of 36.6 mm (794.8 mm^2 area). From tables for overhead aluminum conductors, this conductor has maximum dc resistance of 0.03628 ohms/km at 20 deg C. It has continuous current rating of 900 amperes in moderate temperature. The remaining 4 sections, F*3 to LM*6, and F*3 to F*4, are made from stranded aluminum conductor with total nominal diameter of 17.7mm (186.0 mm^2 area). From tables for overhead aluminium conductors, this conductor has maximum dc resistance of 0.1547 ohms/km at 20 deg C and continuous current rating of 400 amperes in moderate temperature. The overhead power lines are installed on a single pole structure carrying all three phase conductors on single crossarm per pole with 1.2 meters apart horizontally. Vertical height of each conductor at towers from ground is 14 meters and at mid span is 10 meters. Distribution lines are normally untransposed and without earth wire. The three phase system is named as ABC, with the B phase in the middle. Average earth resistivity is typically 300 ohms-m.

To facilitate EMTP Simulation, the system is considered earthed at both ends, the source and the load. The EMTP requires the phase voltage of the source EMF ($11/\sqrt{3}=$) 6.351 kV. Accordingly the peak voltage value is 8.9815kV at source. The source is considered as an ideal voltage source with internal impedance of (0.1+j1.0) Ω per phase (MVAsc = 100).

For the sake of simplicity in simulation, 15 conductor nodes are given names in addition to the unnamed 4 earth nodes. This is for the 13

section line. This is made available on each conductor. The (*) notation for each node name shown in the single line diagram represents any of the three letters A,B,C to represent the corresponding phase of the three phase conductors. The distribution system described in this thesis uses Standards followed by SWEB, as shown in Appendix A. Out of 19 nodes, 6 node names (L1* to L6*) will be converted into 12 single node names to accommodate the fault locators.

Considering a temporarily high load condition for the three 3-phase loads 20MVA, 10MVA, and 10MVA, at 0.8 p.f. & 11kV, these are located at nodes N*, LM*6 and F*4 respectively. Thus total feeder load is 40MVA. Using per phase load ratings (i.e. 6.67MVA at N* and 3.33MVA at LM*6 and F*4) and with the per phase voltage of 6.351 kV, the load impedances, from basic equation $VA_{ph}=(V_{ph}.V_{ph})/Z_{ph}$, are Z_{L1} = (6.351*6.351)/6.67 = 6.05 ohms, and Z_{L2} = Z_{L3} = (6.351*6.351)/3.33 = 12.1 ohms. When converted into their respective resistances and inductances these impedances become Z_{L1}= 4.84+j3.63 & Z_{L2}=Z_{L3}=9.68+j7.26 ohms. Load impedances are shown in fig 2.1.

To improve the study, a capacitance C typically of 0.12uF, shown in figure 2.1 in parallel with the load at LM*6, represents bushing and winding capacitance of a step down transformer.

2.2 Installation Of Capacitor Banks

All loads and distribution lines contribute inductive component of current which reduces the capacity of generating system and power lines. They also increase line losses over conductor resistance. To reduce running copper loss and virtually increase capacity of the power system, capacitor banks [34] are installed at load centers. Their rating is selected to improve the power factor (p.f.) of the individual load to near unity (see Figure 2.2). To achieve this p.f., there are two approaches, (a) to install capacitors exactly at load sites (see figure 2.3), or (b) to install single capacitor bank at location which gives maximum improvement to a maximum possible number of loads (see figure 2.4). This will also improve the voltage profile over the feeder. Both approaches will be used for the analysis given in chapter 8, to study effect of capacitors on performance of fault locator.

2.3 Calculating the Capacitance of the Bank

Figure 2.2 shows a generalised single phase inductive load in shunt with a capacitor bank for p.f. improvement. For unity p.f., reactive component of the two parallel branches (inductive load & capacitor bank) should be equal to zero. The total parallel branch impedance Z of the load and the capacitor bank is given by equation 2.1.

$$Z = \frac{(R + j\,X)\,(jX_c)}{R + j\,(X + X_c)} \qquad (2.1)$$

Solution of equation 2.1, gives equation 2.2.

$$Z = \frac{-R.X.X_c + j\,X.X_c(X+X_c)}{R^2 + (X+X_c)^2} + \frac{j\,R^2.\,X_c + R.X_c(X+X_c)}{R^2 + (X+X_c)^2} \qquad ----------(2.2)$$

Separating real & imaginary terms of equ. 2.2, gives equations 2.3 & 4.4.

$$Z_R = \frac{-\,R.X.X_c + R.X_c(X+X_c)}{R^2 + (X+X_c)^2} \qquad ----------(2.3)$$

$$Z_I = j\,\frac{X.Xc(X+Xc) + R^2\,.\,X_c}{R^2 + (X+X_c)^2} \qquad ----------(2.4)$$

As the imaginary component of the parallel branch impedance is zero at unity p.f., substituting $Z_I = 0$ into equation 2.4, and solving the resulting equation, gives equation 2.5.

$$0 = X.X_c.(X+X_c) + R^2\,.\,X_c \qquad ---------- \qquad (2.5)$$

Solving equ. 2.5 for capacitive reactance X_c, equ. 2.6 is obtained, in which X_c is expressed in terms of load resistance R and load reactance X.

$$X_c = -\,X - \frac{R^2}{X} \qquad ---------- \qquad (2.6)$$

Now substituting the value of inductive reactance X=7.26 ohms (for L=23.1093 mH) and R=9.68 ohms into equation 2.6, it gives X_c= -20.167 ohms. From the value of X_c, the capacitance C is 157.8396115 uF. Table 2.1 shows three phase load ratings, single phase load impedances along with

corresponding single phase values for shunt capacitor banks used in the network.

As there are three 3-phase inductive loads, three separate 3-phase capacitor banks are required to improve p.f. of the system loads to unity, as shown in figure 2.3 of the distribution network. For convenience of maintenance and protection from surges, all the three 3-phase capacitor banks are desired to be installed at one place, equally close to all the loads. The suitable place for such a single giant capacitor bank is at F*2, as shown in Figure 2.4. The value of total per phase capacitance at F*2 is equal to sum of the individual capacitances at three loads in shunt, which comes out to be C_t= 631.3584451 uF (X_{ct}=-j 5.041666721 ohms) per phase. The rating of this single-phase capacitor bank at 6.351 kV phase voltage is ($V_{ph}.V_{ph}/X_c$=) 8MVAR. This sums up to (3x8=) 24MVAR total capacitance of the three capacitor banks at F*2 required for all three 3-phase loads of 40 MVA distributed at 3 locations.

Table 2.1
Details of loads and capacitor banks on the 11 kV system

Load Name	3-PH Load Rating at 11kV,.8 pf	Load Imped in ohm	Load Induct in mH	Capaci of bank uF/ ph	3-PH Rating of Capacitor bank
N*	20MVA	ZL1=4.84+j3.63	L1=11.56	C1=315.68	12MVARc
LM*6	10MVA	ZL2=9.68+j7.26	L2=23.11	C2=157.84	6MVARc
F*4	10MVA	ZL3=9.68+j7.26	L3=23.11	C3=157.84	6MVARc

2.4 Description of EMTP Simulation Program

EMTP is one of the softwares for the simulation of power system transient problems [35]. It is capable of giving the transient solution for a power network under predefined conditions.

The EMTP is probably famous for transmission line switching and transient studies for its multi-choice representation of the power system, i.e. distributed or lump line parameters for the overhead lines and cables. Selection of the time step (δT) depends upon object of simulation and type of the subroutine representing the line parameters. The EMTP has an version takes account of the frequency dependent line parameters with its distributed nature and that is of J Marti. If the transient fault is

of a long duration (several milli-seconds type) such as line to earth or line to line fault, then time step required can be up to one tenth of a millisecond. This is inspite of the fact that a small improvement in results may be obtained by reducing the time step further. If the object of simulation has very short time, as for lightning arcs, then the program requires a time step in the order of nanoseconds. If subroutine JMARTI is selected for representing the distributed line parameters for a short line length then the main EMTP program does not run until the time step is corrected to reduce it to a microsecond, the exact value depends upon length of line and other characteristics of the program. Lightning arc simulation requires very small time step of nanoseconds as the impulse causing power line faults is in itself only of few microseconds duration. Any time step size greater than 20 nanoseconds may produce wrong results.

2.5 Steady-State Behaviour Of The Distribution Network

In order to study, steady-state and transient behaviour of the selected network, there can be no better time than presenting it in this chapter. The smooth 50 Hz sinusoidal & periodical waveshape of the steady-state voltage and current at the source and the load, simulated by the EMTP, and confirmed by manual calculations (if any), is clearly the way to confirm the accuracy of the EMTP program and its success in simulation of the results.

The successful EMTP steady-state results and method of simulation confirms accuracy of both steady-state and transient results because the steady-state EMTP results are obtained from transient solution but skilfully by using a very high fault resistance of 99.0E+90 ohms in place of the short circuit (figure 2.5).

Using the EMTP version JMARTI which is based on the travelling waves over the distributed line parameters, the selected distribution network, shown in figure 2.5, is simulated for the steady-state results using a time step δT equal to 4.5 μ sec. The results are shown in figures 2.6 to 2.15. Curves 1 & 2 in figure 2.6 show phase A voltage and current of the supply source A. Phase B & C source voltage and current are not shown here because they are similar in shape and magnitude except that

they lag phase A by 120 and 240 degrees respectively. The peak value of the source voltage and current in each phase, as shown in figure 2.7, are 8981.46 (= 6351.0 rms) volts and 1295.6 (= 915.70 rms) amperes respectively. Curves 3 & 4 in figure 2.8 show the voltage and current of the A-phase for the load ZL1 at node NA. Phase B and C are checked but not shown here for brevity. The peak load voltage and current value, as measured from figure 2.9 are 5492.0 (=3883.42 rms) volts and 907.7 (= 641.84 rms) amperes respectively. The waveshape shows that the current is lagging the voltage at 0.8 p.f. Dividing rms voltage value at terminal NA (3883.42 volts) by the terminal load impedance $|ZL1| = 6.05$ ohms, the rms value of the current is 641.88 amperes. The manual calculation of 641.88 ampere is same as computer current of 641.84 rms amperes. This manual calculation proves that the EMTP results are accurate. Curves 5, 6, 7, and 8 of figures 2.10 and 2.12 show the load voltage and current at nodes FA4 & LMA6 respectively. Their peak values are shown in figures 2.11, and 2.13. Table 2.2 shows the summary of steady-state voltages and currents at different nodes in the network. It also shows steady-state no load voltages and currents for the sake of comparison with the corresponding loaded values. The noload voltages are obtained without capacitor banks. The noload terminal voltages for phase A are plotted in the set of figures 2.14 to 2.15. Figure 2.14 shows various no load terminal voltages. Due to the large scale used in this figure, these terminal voltages look the same. However when expanded, these voltages (not shown here) have slight differences. Figure 2.15 shows no load source current in phase A. The noload terminal voltages are slightly higher than source voltage due to mutual capacitance between lines and the earth. The noload terminal voltage LMA6 is higher than other voltages, due to the added terminal capacitance of 0.12 uF. As these voltage and current computations are accurate, these curves show that the simulated results are surely accurate for the network shown and that EMTP is a reliable method of fault simulation.

Table 2.2
Summary of steady-state voltages & currents at diff. nodes.

	per phase Load supply values				per phase No-load values			
Node name	peak cur. amp.	rms cur. amp.	peak votage kV	rms vol kV	peak cur. amp.	rms cur. amp.	peak volta. kV	rms volta. kV
JDGA	1295.6	915.70	8.98	6.35	0.9	0.64	8.9815	6.35
NA	907.7	641.84	5.492	3.88	0	0	8.9845	6.35
FA4	423.3	299.32	5.122	3.62	0	0	8.9848	6.35
LMA6	423.3	299.32	5.123	3.62	0	0	8.9855	6.35

2.6 Transient Behaviour Of The Distribution Network

Simulation of transient behaviour of the selected distribution network for a fault at YARB (see figure 2.5), is required for two reasons (i) to confirm suitability of EMTP Programs, and (ii) to establish the difference between the results obtained from similar programs in the coming chapters when fault locators are simulated. A program based upon travelling wave distributed line JMARTI parameters is executed. For B-phase solid earth fault at YARB, the fault transient results are shown in Figures 2.16 to 2.24. Fault transient voltages and currents shown in these figures, show that the transients are neither high in magnitude nor long in duration. To produce high transients, light or no load with fault occurrence near peak voltage value is required. Magnitude of source phase voltages, as shown by curves 1, 3, and 5 in figures 2.16, 2.17 and 2.18 respectively show that the magnitude of transient source voltage in each phase is the same as that of the corresponding steady-state phase value. The source current drawn by the faulty phase B, as shown in figure 2.17 by curve 4, is greater in magnitude than that of the remaining phases shown by curves 2 and 6 in figures 2.16 and 2.18 respectively. Phase voltage of the earthed node suddenly drops to zero value (see figure 2.19), but the fault current of the faulty node to earth increases from zero to a significant value depending upon the line impedance between the faulty node and the corresponding source. Figure 2.20 shows phase A and phase C voltages on nodes YARA and YARC parallel to the fault node YARB. Voltages and currents at other nodes on both sides of the fault are shown in figure 2.21 to 2.24. Voltage curves in these figures show that

sufficient voltage is induced from phases A and C into phase B and therefore voltage in all nodes on either sides of the fault (at YARB) increases as line progresses. Figure 2.21 shows phase A and phase C voltages and currents at nodes FA2 and FC2 of the capacitor banks. Fault B-phase voltage and current for node FB2 of the capacitor bank is shown in figure 2.22. The B-phase voltage at FB2 node shows that the voltage has been induced to the B-phase from the healthy A and C phases. Figures 2.23 and 2.24 show voltages and currents at load terminal N*. The terminal load voltage, shown by curve 21 in figure 2.24, shows that its peak value at a certain time has gone beyond 6kV. Thus both load current and voltage in the faulty phase B are non-zero at all nodes away from the fault.

Chapter-3

GENERAL BEHAVIOUR AND INSTALLATION OF THE FAULT LOCATOR

3.1 Requirements of a fault locator

A fault locator is a complete system or a device which localises system fault to its exact location in a distribution system, as soon as it occurs. A perfect fault locator which operates by fault transients, must be;

1. Fast in operation to avoid circuit breakers interrupting transients.
2. Independent in operation (i.e. must not operate by unwanted signals, frequencies or power supply except by assigned signals and frequencies).
3. Regional in operation (i.e.must not operate if the fault is outside its region)
4. Capable of operating on low as well as high level fault transient. This means it should be capable of recording and capturing enough signal from low level fault transient and capable of operating on the low level captured signal.
5. Accurate in operation (i.e. capable of discriminating fault required frequencies from ordinary power frequency, unwanted transient frequencies, and other signals existing in the system)
6. Free from disturbance to other devices and fault locators (i.e. must not hamper operation of other devices, other fault locators or instruments in its region and outside its region.
7. Reliable (i.e. must not maloperate on changes in temperature, climatic and environmental changes such as rain, magnetic fields, broadcasting signals, earth mineral deposits, closeness of a human or his vehicle)
8. Cheap in capital & running costs and near maintenance free.
9. Capable of operating in all distribution systems, voltages, and line configurations etc.

The operation of the fault locator of our research will be judged in light of these requirements of a good fault locator.

3.2. Constructional difference between past and present fault locators

Figures 3.1 and 3.2 show the circuit components of the past [1-9] and present [10,11] fault locators respectively. Complete design principles and procedures of present fault locator will be presented in Chapters 4 and 5. The two fault locators work on same general principle but they widely differ in constructional details. The previous fault locator of Figure 3.1 has single trap circuit, and simple LCR stack tuner whereas present fault locator has twin trap circuit and complex stack tuner. Both fault locators work on a single resonant frequency and a narrow band of frequencies around the resonant frequency. In both cases, the trap and stack tuners are tuned to same resonant frequency and serve the same purposes.

3.3 Reason for the unsatisfactory results of previous fault locators

As shown in Figures 3.1 stack tuner of previous fault locator has a simple series RLC resonant circuit with a constant value of resistance R_0. As bandwidth [36] of series RLC filter is equal to R_0/L, the previous fault locator [1-3] (R_0=500,L=16mH and C=201E-12 Farad)had a bandwidth of 31250 Hertz at center frequency of 90 kHz compared to merely 636 Hz bandwidth of its trap circuit. For a successful operation of a fault locator, on the contrary, it must have narrower bandwidth for the stack tuner than that of the trap circuit. As wideband stack tuner filter was not capable of separating those frequencies which were blocked by the trap circuit from wideband noise frequencies, the stack tuner failed in filtration of wanted fault frequencies from unwanted fault frequencies. As the trap-blocked frequencies formed only a very small percentage of total filtered frequencies, the output of all stack tuners looked the same in magnitude and shape and the fault locator could neither filter them nor work successfully. Only for this reason, external filtration was done in the previous fault locator. The external filtration was done by digital means for three reasons (i) previous researchers could not filter required frequencies by analogue means, (ii) filtration was assumed to be done at a central processing station and (iii) to earn more appreciation and

preferences from future interested manufacturers of this fault locator, as the world trends are going from analogue to digital technology.

Contrary to the previous fault locator design , the present fault locator uses a stack tuner which filters a narrower band of frequencies than that of the trap circuit. By this, it has perfect filtration, and does not require external filtration.

3.4 Installation of fault locator in power distribution network

Figure 3.3 shows distribution network of figure 2.4, with fault locators installed at appropriate places. In this figure, fault locators are installed at unequal distances deliberately for two reasons,(i) for convenience in simulation, as spare nodes will be used for different purposes in chapters 7 and onward, and (ii) to show that the difference in distance between two adjacent fault locators has really no significance on operation of the fault locator. In fact the best place for installation of a fault locator is the pole where it can easily be installed and reached by a utility staff for inspection. In practice the fault locators are supposed to be 0.5 km apart, but here long distances are selected to simulate worst possible condition. Selected distribution system represents a worst possible condition for two reasons, (i) it represents a very long line (having large line voltage drop and line losses) and (ii) it supplies high value 3-phase loads interconnected by radial arrangement (which minimizes level of transients during faults). The author believes if the new fault locator is capable of operating in this worst condition, it will surely work in all situations of any network. For the simulation of power system faults, fault locators are always represented by their equivalent lumped parameters, as shown in Figure 3.3. This circuit represents the basic configuration. Depending upon type of fault, and purpose of study, equivalent circuit parameters (such as capacitance, linear & nonlinear resistances) and devices (such as circuit breakers, arrestors etc) will be connected at proper nodes of this circuit. Simulation of the network for any fault, will be carried out by EMTP travelling wave mode.

3.5 Operating principle of present fault locator (The principle of the trap & stack tuners)

Suppose that the fault occurs at node YARB of the distribution network of Figure 3.3. As soon as the fault takes place, fault noise frequencies are generated at YARB, and travel in both directions along the line away from the fault. The current and voltage created by the noise frequencies induce mutual fault noises in phase A and phase C by expanding and collapsing magnetic and electric fields through mutual inductive and capacitive couplings between the lines.

A single fault locator unit (for example at JDB2 in figure 3.3) is sufficient to detect the travelling wave fault and its direction. A single fault locator unit has one trap circuit and two stack tuners, one stack tuner on each side of the trap circuit. The trap circuit and stack tuners are resonated to same center frequency f_0 and a band of frequencies around the center frequency. The trap circuit rejects or stops the specified narrow band of frequencies where as the stack tuner filters and gets them out as an output signal. As the trap circuit has one stack tuner on its each side, when a fault occurs, noise frequencies travelling from the fault first strike only the one stack tuner which is very close to the fault (and on the side of fault). This stack tuner filters the selected band of frequencies from the wide band noise frequencies. After striking the closest stack tuner, the noise frequencies then strike the trap circuit. All noise frequencies are allowed to pass through the trap circuit except those frequencies which are filtered by the fault side stack tuner. Thus the second stack tuner on the other side of the trap circuit does not receive any of these selected and trapped narrow band of frequencies and therefore the second stack tuner neither could find nor could filter any of these frequencies. Thus in a way the second stack tuner could not filter any output of the trap stopped frequencies or any other frequency. As the stack tuner on the side of fault has high level of filtered signal compared to zero output of the second side stack tuner, the higher output clearly indicates that the fault is on the side of stack tuner with high filtered output. The closeness and direction of the fault are thus identified by high output stack tuner while the second stack

tuner of the same fault locator has a zero or near zero filtered signal.

Usually several fault locators are installed on a single line, starting from first fault locator at the source and the last fault locator at the load terminal. In such situation a fault always happens between two fault locators and that the two fault locators will indicate presence of a fault in a joint area of fault. If the fault locators are installed close enough (i.e. distance between them is minimum), the fault can be located very easily, conveniently, economically, and quickly.

Chapter -4

DESIGN PARAMETERS OF THE TRAP

4.1 Introduction

In chapter 3, the trap was described one of the main components of present fault locator which blocks a required band of frequencies. The present fault locator uses a twin trap circuit. In this chapter, parameters of the twin trap circuit are designed. The twin trap circuit is used in this research for wideband requirement of the present fault locator. As (described later) a twin trap circuit is a series combination of two single trap circuits. Thus designing parameters of the twin trap circuit needs designing parameters of two corresponding single trap circuits. A single trap circuit has 3 parallel branches. Two branches of each single trap circuit form a basic bandstop filter [14,15,36,38,41,42] (which is called two-branch trap in this thesis) while the third branch of the single-trap circuit is used to reduce peak resonant impedance of the two-branch trap circuit, a condition necessary for obtaining smooth and flat characteristics from the twin trap. For this reason design of parameters of the twin trap circuit starts first by designing parameters of the two-branch trap circuit and then converting it into the single trap and finally by converting the single trap design parameters into the twin trap design parameters. In this series of designs, the two branch trap circuit forms a basic trap circuit which when developed becomes the single trap and finally when further developed becomes the twin trap.

To check performance of each trap circuit, impedance-frequency characteristic of the two-branch trap, the single trap and the twin trap are determined separately in each case from their corresponding design parameters. Using same procedure adapted for designing the twin trap circuit for 10 kHz, two more twin trap circuits, using same value of inductance L =0.1mH, are designed for resonant frequencies of 50kHz and

90kHz. Effect of resonant frequencies of 10kHz, 50kHz and 90kHz on bandwidth of their corresponding twin trap circuits is separately determined and then mutually compared from their impedance frequency characteristic drawn over same impedance and frequency axes and then separately. The comparison shows that for higher resonant frequency f_0 the twin trap circuit provides wider bandwidth and vice versa. Finally impedance-frequency characteristic of the two-branch, the single and the twin traps for the same resonant frequency of 10 kHz are compared to confirm increase in the bandwidth of the twin trap circuit.

4.2 Requirements specification of the trap circuit

While the methodology of the trap is an important component to the present fault locator, other equipments and systems [1-15,36-42] have long used the method. These equipments stop a specified bandwidth b of frequencies centred around a resonant frequency f_0 such that the stopped (or trapped) frequencies do not cross the trap circuit to the other side which is in turn connected to different power line or lines. As an example, if noise frequencies are generated by an earth fault on a line connecting two identical traps, then the specified particular bandwidth b of frequencies from f_0-b/2 to f_0+b/2, for which the trap circuits are tuned, will be restricted into an area between them. The specified bandwidth of fault frequencies, therefore, can not be spotted in any other area outside the area bounded by the two identical traps.

From the above explanation and given example, the trap is a device which totally blocks a complete range of frequencies. To block desired signal frequencies, a trap is required to have;

i) A high impedance (preferably constant) in the range of 8k ohms[37-40] and above, over an entire bandwidth of required frequencies. These ohmic values will be confirmed in the following section.

ii) Bandwidth as wide as possible, preferably in the range of 50Hz to 200Hz and in any case not less than twice the bandwidth of stack tuner. Justification of this assumption is given on page 57. If and only if bandwidth of the trap circuit is wider than the bandwidth of stack tuner, the fault locator is capable of locating faults at

their exact location. The wider bandwidth also helps in increased level of signal outputs from this fault locator as described in sections 5.5.3, 5.5.4, 5.5.5 and 7.2.2.

iii) Identical shape, size, magnitude, materials, bandwidth, resonant frequency and other electrical characteristics in all of its units working under same coordination.

iv) Reliable parameters which does not change with time, magnetic and electric fields, magnitudes of current, position with earth and other materials, climatic changes, specially rain, snow and wind etc.

v) Robust, cheap and mechanically strong in construction and electrically capable of withstanding huge short circuit currents for considerable length of time.

4.3 The impedance of line traps

References 37-40 describe the purpose of a trap circuit and value of its impedance at resonance. Moynihan [37] states that "Line traps are used to insert additional impedances at carrier frequencies in a line. The line trap has a minimum of 400 to 500 ohms impedance at plus or minus 5 percent off the resonant frequency over the band of 50 kc to 150 kc. The maximum impedance at the resonant frequency is quite high. At resonant frequency of 100 kc, the impedance is 9000 ohms". In the same paper he suggested 2500 ohms as minimum acceptable resonant impedance. Hamsher [38] confirms the opinion of Moynihan by stating "These traps provide minimum impedances of 400 to 600 ohms over their bandwidth, depending on the inductance of the main coil and associated design parameters. The resonant impedance is between 5000 to 10000 ohms". In the opinion of Johnson [39] minimum value of resonant impedance of the trap circuit is between 2.5 k ohms and 10 k ohms. The AIEE Committee on line traps on page 1048 of reference [40] suggests a simple method of increasing resonant impedance of a trap circuit. The Committee stated "The higher the L/C ratio at a given frequency, the higher the impedance (Z) of the parallel branch trap circuit at that frequency. Thus low Z can be increased by increasing the L/C ratio of tuning circuit".

Based upon personal experience guided by above references, the

author of this thesis felt that an impedance of 8000 ohms is sufficient for a trap circuit of any future fault locator. This minimum value is for cutoff frequencies of the trap circuit which will be used throughout the research reported in this thesis. This is irrespective of impedance at resonant frequency, provided resonant impedance is not less than 8000 ohms. Minimum acceptable impedance at resonant frequency is 8000 ohms and the maximum resonant impedance can go up to any figure.

4.4 Evaluation of the two-branch trap

4.4.1 Parameters of the two-branch trap

A trap (shown in figure 4.1) is basically a parallel resonant circuit [41-42] which is installed in series in a power line [1-11, 36-42] through which specified bandwidth b of (noise or carrier) frequencies are stopped by its action as a band-stop filter. A simple two-branch trap, consisting of inductance L in one branch and capacitance C in second branch (see figure 4.1a),has resonant frequency f_0, given by equation 4.1.

$$f_0 = 1 / (2 .\pi. \sqrt{ L.C}) \quad \text{-------} \qquad (4.1)$$

Impedance of a pure two branch parallel LC circuit is infinite at f_0. Since all inductors do have some internal resistance, therefore practically all two-branch traps do not have infinite impedance at their corresponding resonant frequency. Bandwidth of a two-branch parallel LC circuit is proportional to L/C ratio [40] and depends very little on internal resistance of inductive coil of the trap circuit. Figure 4.1b shows a two-branch practical trap. This trap has distributed resistance of power inductor coil. Resonant frequency of this practical two-branch trap is given by equation 4.2. Figures 4.2 and 4.3 show effect of resistance on bandwidth and resonant impedance of a two-branch practical LC trap circuit respectively. Figure 4.2 shows that the bandwidth remains almost same 7 Hz (3.5 Hz at each side of 10 kHz) for 8 k ohms impedance frequencies for all values of inductor resistance. Effect of different values of internal inductor resistance on bandwidth and resonant peak

impedance from figures 4.2 and 4.3, are summarised in table 4.1. Figure 4.3 as well as the table 4.1 show that the effect of the internal resistance on resonant impedance of the two branch trap is considerable. As shown in table 4.1, resonant peak impedance for the lowest value of internal coil resistance of 1.E-15 ohms is 3.95E+16 and for highest value of internal coil resistance of 0.0005 ohms, the resonant peak impedance value reduces to 78957 ohms. This shows that the resonant impedance of the two branch trap is almost inversely proportional to circuit resistance. The impedance-frequency response of these figures are obtained by using L=0.1mH, C=2.533029uF and different values of resistance in the inductive branch of the resonant circuit over 10 kHz resonant frequency.

$$f_0 = 1 / [\ 2.\pi.\sqrt{\{L.C-(R/L)^2\}}] \quad \text{------} \qquad (4.2)$$

Table 4.1
Summary of two-branch trap for different values of resistance

Curve No.	R ohms	L mH	C uF	Resonant Z ohms	Band width	f_0.
1	1.E-15	0.1	2.533029	3.95E16	7 Hz	10 kHz
2	0.0001	0.1	2.533029	394789	7 Hz	10 kHz
3	0.0005	0.1	2.533029	78957	7 Hz	10 kHz

The bandwidth of a two-branch trap, shown in figure 4.3, can greatly be increased by increasing inductance L[40] of the power inductor coil while capacitance C is decreased to maintain same resonant frequency f_0. Figure 4.4 shows impedance frequency response, obtained for 3 different traps with same centre frequency f_0 of 10 kHz and same R/L ratio of 1 of the power coil but with different values of L. Constant ratio of R/L for the power coil at 10 kHz has been selected from the assumption that all the three power coils belong to same material, same batch number and have same diameter etc and as that the low value of R, as shown in table 4.1 and figure 2.2, does not affect impedance-frequency characteristic of a trap circuit in the selected range of 8 k ohms cut off frequencies. From this assumption ratio of the internal resistance of the power coils to their corresponding inductance remain the same. Table 4.2 shows summary of resonant curves of figure 4.4. These curves show that with higher

inductance, wider bandwidth is achieved and vice versa. As shown in table 4.2, the bandwidth is directly proportional to the value of inductance L. Table 4.2 also shows peak resonant impedance for each coil at 10 kHz. From this table impedance of the first trap circuit using L=0.1 mH is 394789 ohms, the impedance of the second trap circuit using L=0.2 mH is 789569 ohms and the impedance of the third trap circuit using L=0.3 mH is 1184353 ohms. These values show that the trap circuit impedance increases rapidly with increase in the value of inductance L. Since power coil of the trap carries power frequency current, increase in its inductance and resistance increases trap voltage drop, line power loss and reactive component of power. High inductance also decreases the power factor and subsequently the efficiency of the power distribution system.

Table 4.2
Summary of three two-branch traps and their curves for different values of inductances.

Curve No	R ohms	L mH	C uF	Resonant Z ohms	Band width	f_0.
1	0.0001	0.1	2.533029	394789	7 Hz	10 kHz
2	0.0002	0.2	1.26652	789569	15.6 Hz	10 kHz
3	0.0003	0.3	.844343	1184353	23.6 Hz	10 kHz

4.4.2 Effect of f_0 on bandwidth and peak impedance of the two-branch trap

With four different resonant frequencies f_0=1kHz, 10kHz, 50kHz, and 90kHz for a constant inductance of L=0.1mH and assuming the ratio of R/L=1, characteristics of the resulting two-branch trap circuits are determined. Assumption of the fixed ratio of R/L=1 in all four cases of the two-branch trap circuits is considered for two reasons (i) low values of R, as explained in section 4.3.1, table 4.1 and figure 4.2, does not affect impedance-frequency characteristic of a trap circuit in the selected range of 8 k ohms cutoff frequencies and (ii) investigation in this section is aimed specifically to see effect of different resonant frequencies on similar trap circuits having same resistance and inductance values. Figure 4.5 shows frequency-impedance curves of all the four traps on common x-y plane. The 1kHz curve is unable to appear on wide x-y scale. Figure 4.5 helps in comparing relative values of peak impedances at their

resonant frequency. In order to compare relative bandwidth, figure 4.6 is drawn on an expanded y-axis. Figure 4.6 shows that wider bandwidth is achieved with higher f_0 and vice versa. As shown in figure 4.6, the resonant frequency of 1kHz is unable to provide peak resonant impedance of the trap circuit equal to 8 k ohms, minimum for a cutoff frequency. Figure 4.7 for f_0=1kHz, figure 4.8 for f_0=10kHz, figure 4.9 for f_0=50kHz and figure 4.10 for f_0=90kHz show expanded curves of figures 4.5 and 4.6. Table 4.3 summaries the results of the four traps and their curves. Table 4.3 shows that the higher resonant frequency, for same value of inductance, produces higher bandwidth and higher peak impedance. Low resonant frequency of 1kHz could not produce required 8k ohms impedance and therefore bandwidth of this trap is zero. Resonant frequency of 10 kHz is able to give a bandwidth of 7 Hz only. Resonant frequency of 50 kHz gives a bandwidth of 198 Hz. Resonant frequency of 90kHz gives remarkable wideband of 636 Hz. Resonant impedance is also higher for corresponding higher resonant frequency. For resonant frequencies of 1kHz, 10kHz, 50kHz and 90kHz, the corresponding peak impedance achieved, as shown in table 4.3, are 3948 ohm, 394789 ohms, 9869605 ohms, and 31977520 ohms respectively. The peak resonant impedance of 3948 ohms for 1kHz show that it did not reach the minimum value of 8 k ohms impedance required for a cutoff frequency set in section 4.2. For this reason the two-branch trap circuit using L=0.1mH at 1kHz has bandwidth of 0 Hz. Higher bandwidth and higher resonant impedance from higher f_0 for same value of L suggest that higher resonant frequency will produce better results from the fault locator using it.

Table 4.3
Summary of two-branch trap circuit parameters & effect of f_0 on bandwidth and resonant impedance.

Trap	R ohms	L mH	C Farad	Resonant Z ohms	Band width	f_0.
1	0.0001	0.1	2.533029E-4	3948	0	1 kHz
2	0.0001	0.1	2.533029E-6	394789	7 Hz	10 kHz
3	0.0001	0.1	1.013212E-7	9869605	198 Hz	50 kHz
4	0.0001	0.1	3.127197E-8	31977520	636 Hz	90 kHz

4.5 Design of a single trap

4.5.1 Design theory of single trap

To keep resonant impedance close to operational impedance of a trap circuit within its bandwidth a third branch is connected in parallel to a two-branch trap, as shown in figure 4.11. Addition of third branch to a two-branch trap, slightly reduces bandwidth of the trap, as shown in figure 4.12. Curves of figure 4.12 show that the three-branch trap circuit is slightly inferior to its two-branch trap. The three-branch trap will be called single trap in this thesis.

4.5.2 Design procedure adopted for the single trap (see figure 4.11)

1. Select resonant frequency f_0 and experimentally determine L and R of the power coil to be used in the single trap at f_0. From measurements of a proposed trap, the laboratory results of the present research power coil provided at f_0=10kHz L=0.1mH and R=0.0001 ohms.
2. Calculate corresponding C from equation 4.3 (for 10kHz C=2.533029 uF)

$$C = \frac{1}{L} \cdot \frac{1}{(2.\pi.f_0)^2 + (R/L)^2} \quad F \quad \text{----} \quad (4.3)$$

3. Determine average value of surge impedance R_0 at frequency f_0 (for 11kV line R_0 = approx. 400 ohms).
4. Select an initial value of k to start program (any value, say 10).
5. Determine impedance of upper, middle and lower branches of the trap circuit shown in figure 4.11,using predetermined values of L, R, C, R_0, k and f_0 into the equations 4.4,4.5,4.6 and 4.7, given below.

$$Z_U = -j / (w.C) \quad \text{----------} \quad (4.4)$$

$$Z_M = (R + j\,w.L) \quad \text{----------} \quad (4.5)$$

$$Z_L = k.R_0 + j\left(w.L - \frac{1}{w.C}\right) \quad \text{----------} \quad (4.6)$$

where

Z_U, Z_M, and Z_L are the upper, middle and lower branch impedances

$$w = 2.\pi.f_0 \quad \text{----------} \quad (4.7)$$

f_0 = the resonant frequency (10 k Hz)

6. Calculate total impedance of the single trap circuit Z_{trap} from equations 4.8 and 4.9.

$$Z_{UM} = \frac{Z_U \cdot Z_M}{Z_U + Z_M} \qquad (4.8)$$

$$Z_{trap} = \frac{Z_{UM} \cdot Z_L}{Z_{UM} + Z_L} \qquad (4.9)$$

where
Z_{UM} is total combined impedance of the Z_U and Z_M respectively.
Z_{trap} is total trap circuit impedance of all the three impedances.

7. Check the value of Z_{trap} which should be lower than the value of impedance for cutoff frequencies of 8k Ω, between 6k Ω & 7.9k Ω. This low value of Z_{trap} is required for starting value of k so that several values of k and corresponding parameters both for the single trap and the twin trap can be determined. As explained in introduction, purpose of designing parameters of a single trap circuit is to use its design technique in designing parameters of a twin trap circuit to reduce peak resonant impedance and increase bandwidth, essential to achieve flat impedance-frequency response of the twin-trap. Using Z_{trap} (say=6kΩ), determine k.
8. Record the value of k and other circuit parameters from this design.
9. Determine impedance frequency response of the designed three-branch trap using recent value of k and other parameters from same program, plot the impedance-frequency curve, as shown in figure 4.13.
10. Increase slightly value of the k computed in step 7 while keeping all remaining trap parameters same, and repeat step 9.
11. Repeat step 10 as many times as required (for convenience only 4 selective values of k and corresponding parameters are discussed here), each time using different value of k such that peak impedance Z_{trap} of the first curve is approximately at 6 k ohms and of last curve is at least near 12 k ohms.
12. Draw a straight line through 8k ohm as shown in figure 4.13.
13. Select a suitable curve which has low value of peak resonant impedance and maximum bandwidth at 8k ohms cutoff frequencies. As these two

requirements are opposite to one-another a compromise between the two is made to select a curve. Write down values of all parameters of the selected curve of the single trap design parameters.

In present research, for 10 kHz curve 3 of figure 4.13 proves suitable for the single trap design. The value of k for curve 3 is 29.12 and the value of Z_{trap} at resonance is 11314.18 ohms, which is 1.414 times 8k ohms. This curve is selected for the single trap to provide reasonable bandwidth. If a curve with Z_{trap} equal to just 8k ohms is selected, it would have 0 bandwidth, as can be understood from curve 2 of figure 4.13. Figure 4.13 shows 4 curves for k=15, 20, 29.12, and 100 respectively. Peak resonant impedance of curves 1 and 2 have their corresponding resonant impedances less than or equal to 8 k ohms, but as we will see in the following section, curve 1 will be suitable for the twin trap circuit for producing straight (flat) impedance-frequency curve over its cutoff frequencies. Curves 1 and 2 in single trap circuit for 8k ohms cutoff frequencies are unsuitable, as they provide zero bandwidth compared to the remaining curves. As will be shown in next section, curve 2 for k=20 provides better compromised design parameters for a twin-trap. Curve 4 for k=100 has very high resonant impedance, and is slightly wider in bandwidth than others. Although it gives a very high peak resonant impedance at and around resonant frequencies, it is unable to produce the required smooth and approximate straight impedance-frequency characteristic over the cutoff frequencies and therefore can not be considered either for single trap or twin trap circuits.

4.6 Design of a twin trap

4.6.1 Design theory of a twin trap

As explained in section 4.5, a single trap circuit is designed with success. However its bandwidth for f_0=10kHz is still well below the required bandwidth for efficient operation of a fault locator. To increase bandwidth of a bandstop single trap filter, two or more similar traps, each one having its own resonant frequency, can be combined in a systematic way in series to give a smooth wide bandstop filter with a new

resonant frequency equal to average of their previous individual resonant frequencies and a flat impedance-frequency characteristic over a wide bandwidth. Twin trap circuit has successfully been used during this research work [10,11], for its relatively wider bandwidth over single trap [1-9]. A twin trap, as shown in figure 4.14, in fact uses two single traps in series, in which, one trap has higher resonant frequency f_h than the central resonant frequency f_0 and the other trap circuit has lower resonant frequency f_l than f_0 such that the f_0 is average sum of f_h and f_l.

4.6.2 Design procedure for twin trap

1. Select two (if possible identical) power coils having L_1, R_1 and L_2, R_2 as their total inductance and resistance respectively at centre frequency f_0 (10 kHz in present case).
2. As twin trap circuit has two separate single trap circuits, with their centre frequencies f_h and f_l, one above and one below centre frequency f_0, design starts with assumed separation between f_h and f_l by a small **SEParation** of frequencies in Hertz related by equations 4.10,4.11 and 4.12 given below.

$$f_h = f_0 + SEP / 2 \quad \text{----------} \quad (4.10)$$

$$f_l = f_0 - SEP / 2 \quad \text{----------} \quad (4.11)$$

where

$$SEP = f_h - f_l \quad \text{----------} \quad (4.12)$$

3. Select any positive value (say 10 Hz) for **SEP** and determine f_h and f_l from above equations.
4. Determine C_l and C_h from equation 4.3.
5. Select the lowest value of k from single trap design parameters which produces Z_{trap} of the single trap circuit equal to 6 k ohms. This value of k is 15 and it is selected to produce an straight line impedance-frequency characteristic over cutoff frequencies in the twin trap. Using this value of k, determine total impedance Z_{12} of the twin trap for f_0 from equations 4.13 to 4.19 given below.

$$Z_{1UM} = \frac{(R_1 + j\,w\,L_1)\left(\frac{-j}{w\,C_1}\right)}{R_1 + j\left(w\,L_1 - \frac{1}{w\,C_1}\right)} \quad \text{------} \qquad (4.13)$$

$$Z_{1L} = k.\,R_0 + j\left(w\,L_1 - \frac{1}{w\,C_1.}\right) \quad \text{----} \qquad (4.14)$$

$$Z_1 = \frac{Z_{1UM} \cdot Z_{1L}}{Z_{1UM} + Z_{1L}} \quad \text{----------} \qquad (4.15)$$

$$Z_{2UM} = \frac{(R_2 + j\,w\,L_2)\left(\frac{-j}{w\,C_2}\right)}{R_2 + j\left(w\,L_2 - \frac{1}{w\,C_2}\right)} \quad \text{------} \qquad (4.16)$$

$$Z_{2L} = k.\,R_0 + j\left(w\,L_2 - \frac{1}{w\,C_2.}\right) \quad \text{----} \qquad (4.17)$$

$$Z_2 = \frac{Z_{2UM} \cdot Z_{2L}}{Z_{2UM} + Z_{2L}} \quad \text{----------} \qquad (4.18)$$

$$Z_{12} = Z_1 + Z_2 \quad \text{----------} \qquad (4.19)$$

6. If the value of Z_{12} at 10 kHz is less than 8k ohms, reduce the value of SEP, and repeat steps 4, 5 and 6. If the value of Z_{12} is greater than 8k ohms, increase the value of SEP and repeat steps 4, 5 and 6.
7. Repeat step 6 for Z_{12}, as many times as required, till a suitable value (equal to 8k ohms) is achieved. Record the value of f_l, f_h, C_l, and C_h.
8. Increase value of k by a small value and repeat steps 1 to 7. Repeat this procedure for different values of k.
9. When all curves for different values of k, above and below the value of k suitable for the single trap impedance-frequency characteristic (i.e. k=29.12) are plotted, as shown in figure 4.15, then select suitable curve and note down corresponding values of R, L, C etc. Note that curve 1 for k=15 in figure 4.15 produces nearly straight line impedance-frequency characteristic, but it has lowest bandwidth in all the four curves shown. An increase in bandwidth is obtained by increasing value of the k. As a compromise between straight line (flat)

impedance-frequency characteristic and wide bandwidth, curve 2 for k=20 is the best selection for 10 kHz resonant frequency. The design parameters for this curve are $L_1=L_2=0.1$mH, $R_1=R_2=0.0001$ ohms, $C_l=2.535021$ uF, $C_h=2.531040$ uF, $R_0=400$ ohms, $f_h=10003.93$ Hz, $f_l=9996.07$ Hz, **SEP**=3.93 Hz and k=20. However, for simplicity in future calculations, this curve will be considered for k=20 and **SEP=4.0 Hz** (instead of **SEP**=3.93 Hz) and the corresponding values of C_h and C_l equal to 2.531004 uF and 2.535057 uF respectively, as shown in table 4.4. Figure 4.15 shows that the total bandwidth is, in average, from 9991.5 Hz to 10008.5 Hz. This provides a total bandwidth=17Hz of the twin trap for 10kHz resonant frequency.

4.6.3 Characteristics of the Twin trap at different f_0 frequencies

Using design procedure of section 4.5.2 for f_0=10kHz, for common parameters of $L_1=L_2=0.1$ mH, $R_1=R_2=0.0001$ ohms and k=20, the twin trap circuit parameters (i.e. capacitance) for resonant frequencies of f_0 equal to 50 kHz and 90 kHz are designed. The impedance-frequency characteristic of these designed trap parameters are shown in figure 4.16 and summarised in table 4.4. These curves show that higher bandwidth is achieved at higher resonant frequency f_0 and vice versa. For same value of inductance $L_1=L_2=0.1$mH, f_0=10 kHz provides total bandwidth of 17 Hz, f_0=50 kHz provides bandwidth of 391 Hz and f_0=90 kHz provides bandwidth of 1273 Hz. These bandwidths for ease in comparison are shown in table 4.4. Higher bandwidth for higher resonant frequency (for same value of inductance) shows that the use of high resonant frequency in trap circuits would be beneficial for the over all performance of the fault locator.

Table 4.4
Summary of twin trap parameters & characteristics for different f_0 using constant inductance, resistance & k.

Trap No	f_0 kHz	SEP Hz	C_h Farads	C_l Farads	BW Hz	Resonant Impedan	Z_{max} ohms
1	10	4	2.531004E-6	2.535057E-6	17	8000	9443
2	50	96	1.009332E-7	1.017114E-7	391	8100	10240
3	90	318	3.105215E-8	3.149414E-8	1273	8002	10186

4.7 Comparison of the bandwidth of the twin trap versus single trap and two-branch trap

Performance of a trap circuit is proportional to its bandwidth. To compare performance of various types of traps, their bandwidth is compared for common resonant frequency f_0. Figure 4.17 shows impedance-frequency characteristic of two-branch, single and twin traps obtained by using L=0.1mH, R=0.0001 ohms, and f_0=10kHz. These curves show that the bandwidth of the twin trap is twice wider when measured between the cutoff frequencies over the 8k ohms impedance line than single trap or two-branch trap. This ensures that use of twin trap circuit is surely beneficial to improve fault locator performance.

Chapter-5

DESIGNING THE STACK TUNER

5.1 Minimum Requirements of Stack Tuner

A stack tuner, as the trap circuit, is also an important part of the fault locator which helps in the detection and identification of fault presence and that is by filtering a specified band of fault noise frequencies through the stack tuner impedance which is equal to the line surge impedance. First requirement of stack tuner is to produce its circuit impedance equal to the surge impedance of the distribution line at resonant frequency so that non or very little reflection or scattering of specific frequency waves take place. Second requirement of stack tuner is to keep its bandwidth narrower than that of trap so that the bandwidth of the stack tuner is well within the bandwidth of the trap circuit at same resonant frequency f_0. This is desired for perfect filtration and identification of fault frequencies. Third requirement of stack tuner is that its resonant frequency is the same as the resonant frequency of the trap circuit of the same fault locator. If any of these three requirements is not fulfilled, the fault locator may not operate successfully.

5.2 Constructional difference between previous & present stack tuners

Figures 5.1a and 5.1b show the previous [1-9] and present [10,11] stack tuners respectively. Although their purpose is the same, they are quite different in construction and response. Both of these will be designed and studied in detail in this chapter. For the same f_0 and C, the value of L is the same in both cases. R_0 of figure 5.1a of series stack tuner is replaced by parallel combination of C_n, L_n & R_n of series/parallel stack tuner. If resonant frequency of series LC components in series/parallel stack tuner is f_0, then C_n, L_n and R_n of parallel stack tuner are also tuned to f_0.

As present research is a continuation of previous research, present research is carried, like previous fault locator, on market available stack tuner capacitor C=70pF. Studies of the previous fault locator show that it used the stack tuner capacitor of 201pF for f_0=90 kHz and it was not successful in operation. This was attributed to the poor design which caused interference with other communication frequencies (wireless). Effectively the old fault locator frequency of 90 kHz was within the wireless band and needed reduction. As will be shown at a later stage in this chapter, a series LCR stack tuner as used in the previous fault locator needed a low value of capacitance,about C=1pF, not realised by the previous works. Instead a stack tuner capacitor of 201pF was selected for the series LCR stack tuner, which gave stack tuner bandwidth of 32137Hz against a bandwidth of 636 Hz of the trap circuit. As bandwidth of stack tuner was more than the bandwidth of the trap circuit, the stack tuner failed to filter wanted frequencies from the unwanted. Consequently the old fault locator had to be improved.

In the present fault locator, a stack tuner capacitance, when measured on available fault locator is found 70 pF. A series LCR stack tuner capacitance C=2pF or less is required for a successful operation of this fault locator with series LCR stack tuner. Since this value of capacitance is not available, changes in design of the stack tuner are made, as shown in figure 5.1b. However for the sake of design investigations and future applications, fault locator with series LCR stack tuner (figure 5.1a) will be designed and tested for its performance.

5.3 Design parameters & performance of series LCR stack tuner

5.3.1 Use of series LCR circuit as bandpass stack tuner

Figure 5.2 shows a series LCR circuit. This circuit acts as a bandpass filter [14,15,36,38,41,42]. At resonance, X_C cancels X_l (i.e. X_C=X_l) and high value of current flows through R_0. Consequently all voltage drop takes place across R_0. At resonance V_{out}=V_{in}. At off the resonant frequencies, for frequencies much lower than f_0, X_C >> X_l (because at low frequencies, C acts like open circuit and X_C impedance becomes very high) and for frequencies much higher than f_0, X_l >> X_C and

in either case maximum voltage drop takes place across the combined impedance $(X_l - X_c)$ and the voltage drop across R_0 reduces to negligible value. This action provides high gain filtration for specified resonant frequency f_0 and surrounding frequencies. Magnitude of output is given by equation 5.1.

$$v_0 = v_i . R_0 / \sqrt{[(X_l - X_c)^2 + R_0^2]} \quad \text{----------} \qquad (5.1)$$

Bandwidth of series LCR is given by [41] equation 5.2.

$$BW = R_0 / L \quad \text{----------} \qquad (5.2)$$

Thus for higher values of R_0, bandwidth of series LCR circuit is wider and vice versa. For constant value of R_0, the bandwidth of series LCR circuit is inversely proportional to the inductance.

5.3.2 Design of Series LCR Stack Tuner

C of series LCR stack tuner in figure 5.1a and 5.1b is capacitance created by a dielectric between metallic tube holding the overhead conductor and metallic coating held within the fault-locator assembly. This metallic coating is connected in series to lumped inductance L and lumped resistance R_0 equal to surge impedance to complete series LCR stack tuner. Design starts by measuring capacitance C at chosen resonant frequency f_0. Value of L is calculated from equation 5.3,

$$L = 1 \; / \; [(2.\pi.f_0)^2 . C] \quad \text{----------} \qquad (5.3)$$

The value of R_0 is equal to the surge impedance of the distribution line at f_0, which lies between 400 to 500 ohms.

5.3.3 Effect of characteristic impedance R_0 on the bandwidth of the series LCR stack tuner

From equation 5.2, the bandwidth is proportional to R_0. R_0 depends only upon the distribution line parameters and therefore can not be controlled by series stack tuner parameters. For best results, the value

of R_0 of series LCR circuit must be equal to surge impedance of the power line for standing wave phenomenon. As the value of C is fixed by existing fixture, for a fixed constant value of f_0 and C, the obtained value of L from equation 5.3, must also be constant. For this reason in the series LCR stack resonator for a given value of C, f_0 and R_0, the value of the bandwidth is constant. This means that (1) if the value of C is once high, L becomes always low for all values of f_0. (2) bandwidth of series LCR circuit becomes high compared to the trap-circuit. For such situation filtration by series LCR stack tuner can not be achieved to separate wanted frequencies from the unwanted.

5.3.4 Effect of varying f_0, R_0 & C on bandwidth of series LCR stack tuner

For convenience, four values of C (=1pF,2pF, 5pF,& 70 pF), two values of R_0 (=400 ohms and 500 ohms), three values of f_0 (=10 kHz, 50 kHz, and 90 kHz) are selected to study their effect on bandwidth R_0/L. Table 5.1 shows summary of bandwidth for different values of C, R_0 and f_0. In this table Z50 is the impedance of the series stack tuner at 50 Hz. The impedance-frequency characteristic curve for series LCR stack tuner using R_0=400 ohms, are shown in figure 5.3. Figure 5.4 shows expanded impedance-frequency characteristic of figure 5.3 in the neighbourhood of resonant frequency f_0. Table 5.1 shows that (i) for constant values of R_0 and C, narrower bandwidth is obtained by lowering resonant frequency f_0, and (ii) for constant value of R_0 and f_0, narrow bandwidth is achieved by lower value of C. Reduction in f_0 of the series LCR stack tuner, to achieve narrower bandwidth, will have similar reduction effect on bandwidth of the trap circuit as both operate on the same resonant frequency f_0. As explained in section 4.3.2, reduction in f_0 of the trap reduces both bandwidth & peak value of resonant impedance, making it much inferior. This warns us that better design can not be achieved by lowering f_0 value. Thus the only option left to a designer of a fault locator using series LCR stack tuner, is to reduce the bandwidth of the stack tuner, and that is by reducing the capacitance (C=70 pF) to C=1-2 pF range. The latter can be achieved by reducing dimensions of stack tuner coating ring and increasing separation between metallic tube and the coating.

Table 5.1

Effect of f_0,C and R_0 on bandwidth of series LCR stack resonator

No	R_0 ohm	f_0 kHz	C_{stack} pF	L_{stack} Heneries	Bandwidth $BW=R_0/L_{stack}$	Z50 ohms
1	400	10	1	253.3029	1.579137	3.183E+9
2	400	10	2	126.65153	3.158273	1.59151E+9
3	400	10	5	50.66059	7.895684	6.366038E+8
4	400	10	70	3.618613	110.5396	45471700
5	400	50	1	10.13212	39.47842	3.183E+9
6	400	50	2	5.066059	78.95684	1.591548E+9
7	400	50	5	2.026423	197.3921	6.366191E+8
8	400	50	70	0.1447445	2763.49	45472800
9	400	90	1	3.127197	127.9101	3.1831E+9
10	400	90	2	1.563599	255.8201	1.591549E+9
11	400	90	5	0.6254394	639.5504	6.366196E+8
12	400	90	70	0.04467424	8953.705	45472830
13	500	10	1	253.3029	1.9739	3.183E+9
14	500	10	2	126.65153	3.947842	1.59151E+9
15	500	10	5	50.66059	9.86960	6.366038E+8
16	500	10	70	3.618613	138.1745	45471700
17	500	50	1	10.13212	49.348	3.18309E+9
18	500	50	2	5.066059	98.69605	1.591548E+9
19	500	50	5	2.026423	246.7401	6.366191E+8
20	500	50	70	0.1447445	3454.362	45472800
21	500	90	1	3.127197	159.887	3.1831E+9
22	500	90	2	1.5653599	319.7752	1.591549E+9
23	500	90	5	0.6254394	799.4379	6.366196E+8
24	500	90	70	.04467424	11192.13	45472830

where
No = case number
R_0 = line surge impedance in amperes
f_0 = resonant frequency
C_{stack} = Stack tuner capacitance
L_{stack} = Stack tuner inductance
B = Bandwidth of the series LCR stack tuner
Z50 = impedance of the stack tuner at 50 Hz

5.3.5 Impedance of series LCR circuit at 50 Hz

Looking at the values of impedance Z50 of the series LCR stack tuner at 50 Hz in table 5.1 and the corresponding family of curves for the impedance-frequency response given in the series of figures 5.3, the impedance at the low power frequency 50 Hz is very high (because series capacitor acts like an open circuit at low frequencies) in the range of 4.0E+7 to 4.0E+9 ohms (see table 5.1). This confirms that series LCR stack tuner takes negligible power frequency current and is safe to use in a distribution network.

5.3.6 Comparison of bandwidth of series LCR stack tuner with bandwidth of trap circuit of same fault locator

Successful operation of the fault locator, using either series LCR stack tuner or series/parallel stack tuner depends upon fulfilment of the

minimum requirements of the stack tuner described in section 5.1. One of the three minimum requirements for successful operation of a fault locator, as described in section 5.1, is to keep bandwidth of the stack tuner narrower than that of its trap circuit. The series LCR stack tuners upto now have been used in the commercially available fault locators as well as in the previous researches. For the importance given to these series LCR stack tuners, they were designed in the last section and are summarised in table 5.1. In order to determine usefulness of the designed series LCR stack tuners of table 5.1, their bandwidths need to be compared with the trap circuits designed in chapter 4. In this section bandwidths of the series LCR stack tuners are compared with bandwidth of corresponding trap circuits which can form same fault locators. Criteria for successful operation of the fault locator, used in this chapter for checking bandwidth of the series LCR stack tuner is that its bandwidths should be not wider than the bandwidth of the trap circuit expected to form same fault locator.

Combining data of trap circuits from chapter 4 with data in table 5.1 for LCR series stack tuner, table 5.2 is now obtained for both single trap and twin trap fault locators. Readings 1-12 represent single trap fault locators and readings 13-24 represent twin trap locators.

Table 5.2

Bandwidths of stack tuners versus trap circuits of same fault locator

No	f_0 kHz	C_{st} pF	L_{stack} H	BW_{st} Hz $B=R_0/L_{stack}$	C_{trap} uF	(Half BW) trap Hz	BW_{dif} Hz	Working remark for fault-locator
1	10	1	253.3	2	2.533029	3.5	+1.5	will work
2	10	2	126.652	3	2.533029	3.5	+0.5	will work
3	10	5	50.661	8	2.533029	3.5	-4.5	will not work
4	10	70	3.6186	110	2.533029	3.5	-106.5	will not work
5	50	1	10.13212	39	.1013212	99	+60	will work
6	50	2	5.066	78	.1013212	99	+21	will work
7	50	5	2.026	197	.1013212	99	-188	will not work
8	50	70	0.1447445	2763	.1013212	99	-2664	will not work
9	90	1	3.127197	127	.03127197	318	+191	will work
10	90	2	1.563599	255	.03127197	318	+63	will work
11	90	5	0.6254394	639	.03127197	318	-321	will not work
12	90	70	0.04467424	8953	.03127197	318	-8635	will not work

Table 5.2 continued

No	f_0 kHz	C_{st} pF	L_{stack} H	BW_{st} Hz $B=R_0/L_{stack}$	C_h uF	C_l uF	(Half BW) Hz	Remark on working of fault-loct
13	10	1	253.3	2	2.531004	2.535057	7.5	+5.5 will work
14	10	2	126.652	3	2.531004	2.535057	7.5	+4.5 will work
15	10	5	50.661	8	2.531004	2.535057	7.5	-.5 may work
16	10	70	3.6186	110	2.531004	2.535057	7.5	-102.5 not wor
17	50	1	10.13212	39	.1009332	.1017114	196	+157 will work
18	50	2	5.066	78	.1009332	.1017114	196	+118 will work
19	50	5	2.026	197	.1009332	.1017114	196	-1 may work
20	50	70	0.1447445	2763	.1009332	.1017114	196	-2567 not work
21	90	1	3.127197	127	.03105215	.03149414	637	+510 will work
22	90	2	1.563599	255	.03105215	.03149414	637	+382 will work
23	90	5	0.6254394	639	.03105215	.03149414	637	-2 may work
24	90	70	0.04467424	8953	.03105215	.03149414	637	-8316 not work

where
f_0 = resonant frequency
C_{st} = Capacitance of the series LCR stack tuner
L_{stack} = Inductance of the series LCR stack tuner
BW_{st} = Bandwidth of the stack tuner
B = Bandwidth of the stack tuner
C_{trap} = Capacitance of the single trap
Half BW = Half of total bandwidth between 8k Ω impedance cutoff freq.
BW_{dif} = Difference of bandwidth = Half BW - BW_{st}
C_h, C_l = Twin trap capacitance of high & low frequency filter

Table 5.2 shows that bandwidth of series LCR stack tuner, for C=70 pF is wider than bandwidth of its corresponding trap circuit at the same resonant frequency f_0. This difference increases more rapidly at higher frequencies. As explained in chapter 3, proved in table 5.2 and will be confirmed in the coming chapters, fault locator can not operate successfully under such condition. For low values of C=1pF, 2pF in single and twin trap, bandwidth of the stack tuner is narrower than bandwidth of trap circuit and in such situation, fault locator may work successfully. This proves that series LCR circuit, using available values of C=70 pF, is unsuitable for designing fault locator with series LCR stack tuner, unless value of C is reduced to C=1-2 pF only, where fault locator may successfully filter and separate wanted signals from unwanted frequencies.

5.4 Design & performance of parallel LCR stack tuner

5.4.1 Use of parallel LCR as a bandpass filter

A fully described parallel resonant trap circuit acting as a bandstop filter is introduced in chapter 4. This is connected in series with the power line by which a specified band of frequencies is to be stopped.

For a parallel LC circuit to act as a bandpass filter, it should be connected in shunt arrangement [41,42] and signal is collected across this shunt circuit, as shown in figure 5.5. The shunt output voltage is given by equation 5.4.

$$v_0 = [\ v_i.Z\ ] / [\ R+Z\ ] \quad \text{----------} \qquad (5.4)$$

where Z is total impedance of parallel resonant circuit and R is total impedance of internal voltage source V_i and power line. For $Z >> R$, output V_0 is equal to V_i. For $Z << R$, output V_0 is zero. At resonance Z is maximum and very high output voltage V_0 is obtained. At off resonant frequencies, Z is zero and no or negligible voltage is developed across the parallel resonant circuit and output V_0 is zero. This property of the parallel branch makes it a perfect bandpass filter.

For high output, R of figure 5.5a is replaced by LC circuit as shown in figure 5.5b. The series LC impedance (X_l-X_c) is resonated at the same frequency f_0, for which parallel branch is resonated. Values of L and C are selected according to bandwidth requirement. At resonant, series impedance (X_l-X_c) is zero as Z is maximum and consequently filtered output V_0 is maximum $(V_0=V_i)$ across maximum Z. In this way not only output is surely maximum, but also source does not experience any overloading at off the resonant frequencies when Z falls to zero. At off resonant frequencies, series (X_l-X_c) is very high and parallel impedance Z is zero. This produces zero output. Thus series LC circuit helps parallel resonator in filtration, high output and safeguarding of voltage source from overloading at off resonant frequencies.

5.4.2 Unsuitability of parallel LCR as stack tuner

Characteristics of parallel LCR trap circuit were studied in detail in chapter 4, where by it was shown that a trap circuit has negligible impedance at low frequencies. (Negligible impedance of parallel resonator at low frequencies is due to low impedance of inductance. For example inductive reactance of L=0.1mH at 50 Hz is 0.031415926 ohms only.) For a parallel LCR circuit to act as stack tuner, it has to be connected between two power lines or between a power line and earth. As impedance of parallel LCR circuit at 50 Hz (power frequency) is negligible, it short

circuits power lines with which it (the parallel stack tuner) is connected in shunt and 50 Hz current rushes through the shunt short circuit created by the parallel LCR branch. For this reason, the power system becomes faulty and the system becomes short circuited and overloaded. Consequently a simple and pure parallel LCR circuit can not be designed and used for stack tuner. In order to avoid short circuit between two power lines, LC series filter in series must be connected with parallel filter, as explained in previous section 5.4.1. From characteristics of traps, a parallel two branch LCR circuit has (i) a narrow adjustable bandwidth, not affected by filter resistance and (ii) adjustable resonant impedance controlled by filter resistance of inductive branch. These characteristics will be exploited fully in designing series/parallel stack tuner.

5.5 Design and performance of series/parallel stack tuner

5.5.1 Introduction to series/parallel stack tuner.

From the foregoing discussions, table 5.2 and curves of figures 5.3 and 5.4, it is clear that a series LCR resonant circuit has high impedance to low frequencies including power frequency (50 Hz) and a parallel LCR resonant circuit provides narrow controllable bandwidth and impedance of bandpass filter. If the two filters are combined in series, and output is obtained from across the parallel resonant circuit, then both of the required characteristics of a stack tuner are obtained from this combined filter. Figure 5.1b, whose principle is described in figure 5.5b, shows such series/parallel stack tuner. This stack tuner, has proved itself very worthy of use. It fulfils all the three minimum requirements of a successful stack tuner. This stack tuner has two basic filters. L & C form first filter and C_n, L_n, and R_n form second filter which act as dynamic resistance of first filter. Both of the filters are resonated to same frequency f_0 which is also resonant frequency of corresponding trap of same fault locator. Since first filter is series LC circuit, it has zero impedance at and surrounding resonant frequencies, but very high impedance at all remaining off resonant frequencies (i.e. very low as well as very high frequencies). Main purpose of series LC circuit is to provide very high impedance at power frequency 50 Hz (as shown by curves in figure 5.3

and table 5.1) and zero impedance at f_0. The purpose of second filter is to identify fault frequencies at and around resonant frequency f_0 and filter them out by providing circuit impedance equal to surge impedance at resonant frequencies.

5.5.2 Derivation of design equations of series/parallel stack tuner

Designing of series/parallel stack tuner is straight forward. Series LC filter and parallel LCR filter are designed separately. Designing of series LC filter starts from known value of C and f_0 and then calculation of value of L from equ. 5.3 as already explained in section 5.3.2.

The design of the parallel LCR stack tuner requires understanding of its equations. These equations are derived in this section.

From figure 5.1b (or 5.5b) the impedance of parallel stack tuner is given by equation 5.5.

$$Z_{parallel} = \frac{\left[(R_n + j\,w\,L_n)\left(-j\,\frac{1}{w\,C_n}\right)\right]}{\left[R_n + j\left(w\,L_n - \frac{1}{w\,C_n}\right)\right]} \quad \text{------} \qquad (5.5)$$

At resonant frequency f_0, L_n, R_n & C_n are related [41,42] by equs.4.3 & 5.6

$$C_n = \frac{1}{L_n} \cdot \frac{1}{(2.\pi.f_0)^2 + (R_n/L_n)^2} \quad \text{--------} \qquad (5.6)$$

For $R_n \leq L_n$, (R_n/L_n) is very very small compared to $(2.\pi.f_0)$, and (R_n/L_n) can be neglected in equation 5.6 to become equation 5.7.

$$C_n = \frac{1}{L_n} \cdot \frac{1}{(2.\pi.f_0)^2} \quad \text{----------} \qquad (5.7)$$

Rearranging equation 5.7, equation 5.8 is obtained.

$$(2.\pi.f_0)\,L_n - \frac{1}{(2.\pi.f_0)\,C_n} = 0 \quad \text{----------} \qquad (5.8)$$

Substituting equation 5.8 into equation 5.5 at resonant frequency f_0 with $w=w_0$ $(=2.\pi.f_0)$, equation 5.9 is obtained.

$$Z_{parallel} = \frac{(R_n + j\,w_0\,L_n)\left(-j\,\frac{1}{w_0\,C_n}\right)}{R_n + j\,0} \quad \text{---} \qquad (5.9)$$

Solving equation 5.9 and rearranging terms of the resulting equation into real and imaginary terms, equation 5.10 is obtained.

$$Z_{parallel} = \frac{L_n}{C_n R_n} - j \frac{1}{w_0 C_n} \quad \text{------} \qquad (5.10)$$

At resonant frequency f_0, total impedance of the parallel stack tuner is equal to surge impedance, as given by equation 5.11.

$$R_0 = |(Z_{parallel})| = \sqrt{[(L_n/C_n.R_n)^2 + (1/w_0.C_n)^2]} \qquad (5.11)$$

Since $1/(w_0.C_n) << L_n/(C_n.R_n)$, equation 5.11 becomes equation 5.12.

$$R_0 = \frac{L_n}{C_n R_n} \quad \text{----------} \qquad (5.12)$$

Rearranging equation 5.12 for R_n, equation 5.13 is obtained.

$$R_n = \frac{L_n}{C_n R_0} \quad \text{----------} \qquad (5.13)$$

5.5.3 Design procedure of series/parallel stack tuner

Series/parallel stack tuner has two filters, the series LCR filter and parallel R_n C_n L_n filter. The series LCR filter is designed as explained in section 5.3 and start of section 5.5.2. Designing of parallel resonator is explained in this section.

Designing of the parallel resonator starts with a value of L_n, and computation of C_n from equ. 5.7. As value of L_n is unknown and that the ratio L_n/C_n [40] affects bandwidth of the parallel resonator, reasonable low value of L_n has to be selected such that bandwidth of the stack tuner is not wider than bandwidth of the trap circuit. To meet this condition, the best way is to use L_n less than trap's effective value of inductance L_{effect}. L_{effect} of the trap circuit is equal to sum of all series power coil inductances in the trap circuit, as given in equation 5.14. But there exists no simple method of calculating reasonable value L_n, as there exists no such simple equation to relate bandwidth with L_n, particularly when other parameters C_n and R_n are unknown and variable. This problem is overcome by designing a dozen or more stack tuners with different values

of L_n, as given by equations 5.15 and 5.16.

As one of requirement of stack tuner is to have its impedance equal to surge impedance at resonant frequencies, and (as we know) impedance of series LC circuit is zero at resonant frequency, this surge equivalent impedance has to come from parallel resonator only as given by equation 5.12. This requirement is easily achieved by manipulating the values of parameters L_n, C_n and R_n of the parallel circuit. From the experience in chapter 4 and as explained in reference [40], bandwidth of the parallel resonator circuit is proportional to L_n/C_n. In order not to change bandwidth of the parallel resonator, values of L_n and C_n have to remain same and the only parameter which can be changed is R_n, as shown by equation 5.13. Thus finally R_n is calculated by substituting calculated values of L_n and C_n into equation 5.13. In these equations n=1,2,3....upto N=12, gives required number of parallel stack tuner. Adding impedance of series LC stack tuner with each of 12 parallel stack tuner makes a total of 12 series/parallel stack tuners. This arrangement gives a dozen different series/parallel stack tuners. Impedance-frequency curve of parallel stack tuners when drawn with normalised impedance-frequency curve of the trap circuit provides clear distinction between suitable and unsuitable stack tuners. All stack tuners whose curves does not cross or go above impedance-frequency curve of the trap circuit have narrower bandwidth than bandwidth of corresponding trap of a fault locator. For proper filtration, suitable parallel resonator is the one which has a bandwidth equal to half (or less than half) of the bandwidth of trap. For higher filter output, parallel resonator with wider bandwidth can be selected and used. This laborious work is required due to absence of a suitable bandwidth equation for parallel resonator and basic nature of present work. Once such equation is either derived or becomes available, this procedure may not be used.

$$L_{effect} = L_1 + L_2 + \ldots L_m \quad \text{----------} \qquad (5.14)$$

$$L_{small} = \frac{L_{effect} \cdot R_0}{(\text{No. of stacks, } N)(\text{ Min.Impedance of trap, } 8000)} \qquad (5.15)$$

$$L_n = L_{small} \cdot n \quad \text{----------} \qquad (5.16)$$

In order to design several parallel LCR stack tuners, following step by step procedure can be used:-

1. Find total effective inductance of trap circuit, from equ. 5.14.
2. Calculate minimum value of inductance L_{small} for first stack tuner from equation 5.15, using effective inductance from equation 5.14, minimum trap impedance (8k ohms), value of surge impedance (R_0=400Ω) and (No. of stacks) for convenience is 12.
3. Calculate inductance for other stack tuners from equation 5.16.
4. Calculate C_n for each L_n for same f_0 from equation 5.7.
5. Calculate R_n from equation 5.13.

Table 5.3 shows summary of designed parameters of 12 parallel stack tuners at f_0=10 kHz, for single and twin trap fault locators. Readings 1-12 in table 5.3 represent single trap fault locator and readings 13-24 represent twin trap fault locator. Tables 5.4 and 5.5 provides summary of designed parameters of parallel branch resonators for series/parallel stack tuners at 50 kHz and 90 kHz respectively.

Table 5.3
Designed parameters of parallel branch resonator at f_0 = 10 k Hz

No	L_n mH	C_n uF	R_n ohms	BW Hz of C_n, L_n & R_n	Half-BW trap	Fault Locator
1	.0004166667	607.9270	1.713473E-6	0.66	3.5	will work
2	.0008333333	303.9635	6.853893E-6	1.31	3.5	will work
3	.00125	202.6424	1.542126E-5	1.96	3.5	will work
4	.0016666667	151.9818	2.741557E-5	2.71	3.5	will work
5	.0020833333	121.5854	4.283683E-5	3.27	3.5	will work
6	.0025	101.3212	6.168503E-5	3.92	3.5	will work
7	.0029166667	86.84672	8.396019E-5	4.57	3.5	may work
8	.0033333333	75.99088	1.096623E-4	5.24	3.5	may work
9	.00375	67.54745	1.387913E-4	5.88	3.5	may work
10	.0041666667	60.79271	1.713473E-4	6.53	3.5	may work
11	.0045833334	55.26609	2.073303E-4	7.18	3.5	may work
12	.005	50.66059	2.467401E-4	7.84	3.5	may work
13	.0008333333	303.9635	6.853893E-6	1.30	7.5	will work
14	.0016666667	151.9818	2.741557E-5	2.60	7.5	will work
15	.0025	101.3212	6.168503E-5	3.95	7.5	will work
16	.0033333333	75.99088	1.096623E-4	5.25	7.5	will work
17	.0041666667	60.79271	1.713473E-4	6.55	7.5	will work
18	.005	50.66059	2.467401E-4	7.85	7.5	will work
19	.0058333333	43.42336	3.358408E-4	9.15	7.5	may work
20	.0066666667	37.99544	4.386491E-4	10.45	7.5	may work
21	.0075	33.77373	5.551653E-4	11.74	7.5	may work
22	.0083333333	30.39635	6.853892E-4	13.05	7.5	may work
23	.0091666667	27.63305	8.293210E-4	14.35	7.5	may work
24	.01	25.33030	9.869605E-4	15.65	7.5	may work

Table 5.4
Designed parameters of parallel branch resonator at f_0=50 k Hz

No	L_n mH	C_n uF	R_n ohms	BW Hz of C_n, L_n & R_n	Half-BW trap	Fault Locator
1	.0004166667	24.31708	4.283683E-5	16.30	50	will work
2	.0008333333	12.15854	1.713473E-4	32.65	50	will work
3	.00125	8.105694	3.855314E-4	49.10	50	will work
4	.0016666667	6.079270	6.853843E-4	65.40	50	will work
5	.0020833333	4.863417	1.070921E-3	81.60	50	may work
6	.0025	4.052847	1.542126E-3	98.00	50	may work
7	.0029166667	3.473869	2.099005E-3	114.00	50	may not work
8	.0033333333	3.039635	2.741557E-3	130.60	50	may not work
9	.00375	2.701898	3.469783E-3	147.00	50	may not work
10	.0041666667	2.431708	4.283683E-3	163.20	50	may not work
11	.0045833334	2.210644	5.183257E-3	179.60	50	may not work
12	.005	2.026424	6.168503E-3	195.60	50	may not work
13	.0008333333	12.15854	1.713473E-4	32.70	98	will work
14	.0016666667	6.079270	6.853893E-4	65.30	98	will work
15	.0025	4.052847	1.542126E-3	98.00	98	will work
16	.0033333333	3.039635	2.741557E-3	130.50	98	may work
17	.0041666667	2.431708	4.283683E-3	163.00	98	may work
18	.005	2.026424	6.168503E-3	196.00	98	may work
19	.0058333333	1.736934	8.396019E-3	228.50	98	may not work
20	.0066666667	1.519818	1.096623E-2	261.50	98	may not work
21	.0075	1.350949	1.387913E-2	293.50	98	may not work
22	.0083333333	1.215854	1.713473E-2	326.50	98	may not work
23	.0091666667	1.105322	2.073303E-2	359.50	98	may not work
24	.01	1.013212	2.467401E-2	392.00	98	may not work

Table 5.5
Design parameters of parallel branch resonator at f_0=90 k Hz

No	L_n mH	C_n uF	R_n ohms	BW Hz of C_n, L_n & R_n	Half-BW trap	Fault Locator
1	.0004166667	7.505273	1.387913E-4	34.4	159	Will work
2	.0008333333	3.752637	5.551652E-4	106.0	159	will work
3	.00125	2.501758	1.249122E-3	159.0	159	will work
4	.0016666667	1.876318	2.220661E-3	212.0	159	may work
5	.0020833333	1.501055	3.469783E-3	265.0	159	may not work
6	.0025	1.250879	4.996487E-3	318.0	159	may not work
7	.0029166667	1.072182	6.800774E-3	370.5	159	may not work
8	.0033333333	.09381591	8.882644E-3	423.0	159	may not work
9	.00375	.08339192	1.124210E-2	476.0	159	may not work
10	.0041666667	.07505273	1.387913E-2	530.0	159	may not work
11	.0045833334	.06822975	1.679350E-2	582.0	159	may not work
12	.005	.06254394	1.998595E-2	634.0	159	may not work
13	.0008333333	3.752637	5.551652E-2	106.0	318	will work
14	.0016666667	1.876318	2.220661E-3	212.0	318	will work
15	.0025	1.250879	4.996487E-3	317.0	318	will work
16	.0033333333	.9381591	8.882644E-3	423.0	318	will work
17	.0041666667	.7505273	1.387913E-2	529.0	318	may work
18	.005	.6254394	1.998595E-2	635.0	318	may work
19	.0058333333	.5360909	2.720310E-2	741.0	318	may not work
20	.0066666667	.4690796	3.553057E-2	849.0	318	may not work
21	.0075	.4169596	4.496839E-2	957.0	318	may not work
22	.0083333333	.3752637	5.551652E-2	1065.0	318	may not work
23	.0091666667	.3411488	6.717500E-2	1167.0	318	may not work
24	.01	.3127197	7.994379E-2	1275.0	318	may not work

Tables 5.3, 5.4 and 5.5 are constructed from impedance-frequency characteristics of the designed parameters of the parallel resonators by calculating bandwidth frequencies between cutoff frequencies, as explained in section 5.5.4. Purpose of these tables is to put the designed values

of parameters and bandwidth of the parallel resonant circuits along with the bandwidth of the trap circuits at the same place. These tables show that bandwidth of the parallel branch resonator circuit is proportional to L_n and resonant frequency. For same value of L_n, high resonant frequency f_0 provides wide bandwidth and vice versa. Comparison of bandwidth of parallel resonator is done with half bandwidth of the trap circuit and on the basis of this comparison, condition of the fault locator for its successful operation has been assessed.

5.5.4 Bandwidth of the parallel branch of the series/parallel stack tuner

Since there exists no equation defining exact bandwidth of a parallel filter except proportionality given by ref. [40] L/C, the bandwidth of series/parallel filter, is determined from impedance-frequency characteristic of parallel resonator by the usuall definition of bandwidth. Bandwidth of parallel filter is frequency difference between two frequencies on impedance-frequency curve having $1/\sqrt{(2)}$ of peak impedance. In present case, peak impedance of parallel resonator is R_0=400 ohms and therefore bandwidth of series/parallel stack tuner is the frequency difference between two frequencies having impedance of $R_0/\sqrt{(2)}$ =288 ohms on impedance-frequency curve of corresponding parallel resonant circuit. It should be noted that for proper operation of fault locator, bandwidth of parallel branch stack tuner must be half (or less than half) of the bandwidth of trap circuit (measured at 8k ohms impedance). This condition of bandwidth is necessary and must be fulfilled to enable the fault locator to discriminate between wanted signal frequencies and unwanted frequencies. For justification refer to section 7.2.2 (page 57). Tables 5.3, 5.4 and 5.5 and curves in figures 5.6 and 5.7 compare bandwidth of parallel branch filters with bandwidth of corresponding traps, at resonant frequencies 10 kHz, 50 kHz and 90 kHz respectively. Selection of suitable parallel stack tuner is clearly indicated in remark column of each table. For satisfactory design and well before actual fabrication or construction of the fault locator, it is necessary to simulate a transient fault and check performance of the designed fault locator. As explained before, with wider bandwidth, the fault locator output for the same fault is higher, but when bandwidth of the stack tuner increases a certain level, it losses the property of discrimination for

the fault localisation. For this reason these designed values are tested in chapter 7, as a part of the fault locator using short circuit earth fault simulation. As will be seen in chapter 7, the fault locator is capable of using twice the value of L_n designed and shown in table 5.3 for resonant frequency f_0=10kHz.

5.5.5 Selection of appropriate series/parallel stack tuner on the basis of bandwidth.

For practical considerations, stack tuner with bandwidth equal to half of the bandwidth of trap circuit is used. Accordingly out of the dozen parallel stack tuners designed for single and twin traps, whose characteristics are shown in figures 5.6 and 5.7 respectively only one appropriate stack tuner with bandwidth half of trap circuit is to be selected. For single trap as well as twin trap fault locator, curve No 6 for 10 kHz, meets criteria and could be used. Curves with higher number than 6 can be used, but these may not provide suitable filtration. Each of the higher number curve will produce higher filter output but will lack more and more in selectivity of wanted signal from unwanted signals. For f_0=10 kHz and L_1=L_2=0.1mH, trap circuit has total bandwidth of 7 Hz (at 8 k ohm frequencies) and therefore a stack tuner of bandwidth of 4 Hz (at 0.707 of R_0) or below is required for proper operation of the fault locator. A fault locator having narrower bandwidth stack tuner than bandwidth of its trap locates fault successfully. Proof of this and explanation by fault simulation test results are provided on page 57.

5.5.6 Impedance-frequency response of series/parallel stack tuner

Curves (for L_n=0.002083 mH, 0.0025 mH and 0.002917 mH) in figure 5.8 show impedance-frequency characteristic of series/parallel stack tuner for 10 kHz, 50 kHz and 90 kHz respectively for single trap fault locator and curves (for L_n=0.00417 mH, 0.005 mH and 0.005833 mH) in figure 5.9 show impedance-frequency characteristic of series/parallel stack tuners for the corresponding frequencies for the twin trap fault-locator. Curves in these figures show peculiar characteristic of series/parallel circuit, which is very important for creation of perfect filtration. On both sides of resonant frequency f_0, the total impedance first decreases (till parallel

resonator becomes zero) and then increases rapidly. The decrease or dip in impedance is created by decrease in impedance of the parallel circuit of the stack tuner.

Impedance-frequency response on a wide x-axis (from dc to twice f_0) show exactly the same curves as shown in figures 5.3 due to high impedance of series resonator and zero impedance of parallel resonator at off the cutoff frequencies. Very high impedance value of series stack tuner at 50 Hz confirms that it draws negligible power from 50 Hz source.

Chapter 6

STEADY STATE FREQUENCY RESPONSE OF THE NEW FAULT LOCATOR

6.1 Reasons for finding steady-state frequency response

Once the parameters of the trap circuit and stack tuner of a fault locator are calculated, they are combined together to form a proper fault locator and digitally tested before final decision. There are two frequency ranges of interest, (i) low frequency 50 Hz and (ii) resonant frequency f_0 together with the surrounding frequencies. As fault locator is installed on a 50 Hz power system, minimum interference of fault locator on power system should be expected and vice versa. This is important for successful operation of fault locators. For high frequencies at and around resonant frequency f_0, performance of fault locator is reported in this chapter for suitability in fault localisation.

6.2 Circuit arrangement for finding the required response

Figures 6.1a and 6.1b show details of circuit arrangement to test our fault locator. A signal source acting as a fault point creates all frequencies of constant voltage magnitude, 100 volts. Current of all these frequencies flow into circuit towards fault locator. When resonant frequency f_0 and frequencies on both sides of f_0 strike fault locator, for proper operation, fault locator should detect presence as well as site of striking these frequencies.

In chapters 4 and 5, it was established that higher value of f_0. provides wider bandwidth and consequently higher output. In chapter 4, it was also established that twin trap provides wider bandwidth than single trap. To create worst situation for study, single trap and low resonant frequency (f_0=10 kHz) are selected for fault locator in figure 6.1a and 6.1b. This is to present all fault locator cases. Figure 6.1a shows series stack tuner while series/parallel stack tuner is shown in figure 6.1b. Extra branches of stack tuners are inserted to represent surge impedance

of the distribution lines. Only two outputs, one from each side of fault locator are collected by simulation. The outputs from two sides of same fault locator are compared mutually as shown in figures 6.2 and 6.3 for series and series/parallel stack tuners respectively.

Details of the findings of figures 6.2 and 6.3 will be discussed below.

6.3 Main equation for computations & computer results

Figure 6.2 shows two separate results for two different values of stack tuner capacitance C_{stack}=1 pF and C_{stack}=70 pF. Dashed lines represent output from stack tuner of 70 pF capacitance and solid lines represent output from stack tuner of 1 pF capacitance. Maximum output from stack tuner is from the side of frequency generator (i.e. fault side) equal to input voltage, 100 volts. Voltage output curves in figure 6.2 show that bandwidth of voltage-frequency curve 1 for 70 pF fault locator is wider than bandwidth of voltage-frequency curve 3 for 1 pF fault locator. Presence of output from any stack tuner indicates presence of fault on that side. In both the case, output is obtained from both sides of the fault locator. As fault (i.e. high frequency generation) occurs only on one side, for fault localisation only fault side of the fault locator should be able to provide output. Curves 1 and 2 show that fault locator with 70 pF capacitance provides output from both sides and therefore fails in proper fault localisation. Maximum output of second stack tuner is 75% of maximum output (100 V) of first stack tuner. This shows that the fault locator having C_{stack}=70pF capacitance in series LCR stack tuner does not and can not filter wanted frequencies from unwanted frequencies.

Solid line curves 3 and 4 in figure 6.2 represent performance of the fault locator having C_{stack}=1 pF in series LCR stack tuner. Output from one side is very high(100%) compared to output from other side (maximum 2.5%). This shows that fault locator having 1 pF in its stack tuner is capable of separating wanted frequencies from unwanted frequencies. Thus series stack tuner type fault locator works only with very low values of stack tuner capacitance.

Now consider fault locator with series / parallel stack tuner shown

in figure 6.1b. It uses highest available value of stack tuner capacitance of C_{stack}=70 pF. Output results for 12 designed series/parallel stack tuners are shown in figures 6.3a and 6.3b. Output from fault side stack tuner (curves in figure 6.3a) show that output has increased 6 times the input signal for narrowest bandwidth and 1.5 times for widest bandwidth (i.e the highest value of L_n). The second side output away from fault for all the 12 values of L_n, shown in figure 6.3b is negligible compared to fault side output shown in figure 6.3a. This proves that fault locator with series/parallel of the stack tuner is capable of filtering wanted signal from unwanted signal, in addition to amplifying the received signal as required. Amplification of fault side output takes place when negative (or positive) reactive component of Z_p cancels positive (or negative) reactive component of Z_s in (Z_p+Z_s) of equ. 6.1 below.

$$V_l = V_i \ (Z_p/\{Z_p+Z_s\}) \quad \text{----------} \qquad (6.1)$$

where

V_l= voltage from fault side stack tuner across parallel circuit
V_i= signal of fault or signal generator
Z_p= impedance of parallel circuit (L_n, C_n and R_n).
and Z_s= impedance of series circuit C_{stack} (=70 pF) and L_{stack} (3.6186 H)

Output voltage-frequency curves in figure 6.3a show that the output voltage dies rapidly as frequency reduces towards zero. This ensures that output voltage at 50 Hz is negligible.

Chapter 7

PARAMETER RELATED BEHAVIOUR OF THE FAULT LOCATOR

7.1 Introduction

In this chapter, the fault locator will be tested for different design parameters already computed and introduced in chapters 4 and 5 under real load conditions of 11kV distribution system. Since unloaded line transients are higher than loaded line transients, no load fault effect on parameters of the fault locator will also be tested. On the basis of parameter related performance of the fault locator, proper parameters for final use of fault locator will be discussed and selected.

Figure 7.1 shows distribution network of chapters 2 and 3 with fault locator but without capacitor banks. Capacitor banks have been temporarily removed to avoid by-passing of transient travelling waves through their capacitance to earth. Capacitor banks from nodes FA2, FB2, and FC2 are disconnected but later will be returned to the system. This is to get real performance and understanding of fault locator during parameter related testing. If the capacitor banks were not removed, they would have passed transient fault high frequencies to earth. Fault locator problem due to capacitor bank and its remedies will be fully discussed in chapter 8 and after that the capacitors will always be in use.

7.2 Fault-locator testing for different parameters

7.2.1 Procedure of testing

For proper and justifiable testing of fault locator the following procedure is taken :-

i) use interconnected multi-junction tapping or interconnected network system for testing, as it provides chance for testing fault locator under reflection and scattering of waves due to miss-matching of surge-impedance at multi-line junction of a real 3-phase network.

ii) disconnect all capacitor banks from experimental network to avoid by-

passing of transients through their capacitance to earth and disabling closeby fault locators.

iii) when the fault locators are aimed to have d km minimum distance between them under a practical real application, we have used a minimum of 4d distance between fault locators during computer studies. Present fault locator is aimed to have 0.5 km minimum distance between adjacent fault locators. For satisfactory investigations into the fault locator for testing purpose 3.0 km minimum distance is used from fault to closest fault locator on load side and 1.5 km from fault to closest fault locator on source side. Higher distance is necessary to check effect of mutual coupling between conductors at different sides of the locator.

iv) test the fault locator using solid earth fault for the maximum incipient fault voltage. For faults near the voltage peak value it provides maximum signal output voltage amplitudes which are required to differentiate output voltage from different stack tuners. For faults near voltage zero crossing the noise will be negligible and normally the signal output will not be reliable. The latter type is very rare in the system and only occurs during direct switching on to fault, which requires different equipment.

v) create test fault close to multi-junction, as it provides chance for testing effect of junction on reflections and scattering of waves.

vi) test all sets of stack tuner parameters (and if possible add more sets), starting from lowest L_n and increasing its value slowly and steadily step by step. Compare signal output voltages from different stack tuners mutually for same value of L_n. Output from same stack tuner and for different value of L_n and other parameters of the fault locator have also to be tried.

vii) prepare results in table as well as in graphical form for easy comparison of output signals.

7.2.2 Test performance of fault locator

Figure 7.1 shows, sudden solid earth fault at YARB of the selected distribution network and installation of fault locators having series/parallel stack tuners. Table 7.1 shows list of designed parameters

of the fault locator used for testing parameter related performance. Performance of the fault locator for each set of these parameters is determined by simulation of fault transients of the 11 kV distribution network at stack tuner output terminals. Since stack tuner output terminals represent filter terminals, filtered output voltage of 10 kHz frequency is obtained from these terminals. Using each set of parameters, turn by turn, transient behaviour of the complete network is simulated and outputs across parallel tuned circuit of series/parallel stack tuner are obtained for solid earth fault on phase B at YARB. For the sake of simplicity in discussion, phase B is separately shown in figure 7.2. In figure 7.2 fault locators are named Loc1 to Loc6 for easy reference. Figure 7.2 shows that fault has occurred in between fault locators Loc2 and Loc3 but also between Loc2 and Loc5. Parameter related performance results of fault locators with series/parallel stack tuner in figure 7.2 is shown in figures 7.3, and 7.4. Figures 7.3a and 7.4a show fault locator output when the system supplies some load where as figures 7.3b and 7.4b show unloaded conditions. The unloaded output signal voltages are higher than loaded output signal voltages. The results show that output voltage signal from stack tuner increases with increase in L_n value. Peak value of output voltages, for each value of L_n are shown in table 7.2. This table and corresponding results in figures 7.3 and 7.4 show that output from stack tuners close to fault is higher than output from stack tuners away from fault. Peak to peak voltage output ratio of stack tuners of same fault locator is shown in table 7.3. For L_n=1.0E-3 mH, the voltage ratio is 25.90, 21.75 and 61.78 (see figure 7.4) for fault locators Loc2, Loc3 and Loc5 respectively which are very close to the fault. Voltage ratio of fault locators Loc4 & Loc6 away from fault are constant and low (1.03 and 1.2 for both loaded and unloaded conditions respectively). Table 7.3 shows that as L_n increases, voltage ratio of fault locator close to fault decreases. Results of tables 7.2 and 7.3 combined show that although output voltage from filters increases with increase in L_n, it decreases voltage ratio of voltages from two sides of fault locators close to the fault, thus making fault locator inferior at high values of L_n. It is therefore not necessary to have high value of L_n for fault localisation, as voltage ratio decreases with increase in L_n. For fault localisation, minimum value of voltage ratio for a fault locator close to fault should

not be less than 2.0. At L_n=0.02 mH, testing of fault locators show that voltage ratio (see figure 7.3a and 7.3b) from fault locator No.5 close to fault, as shown in table 7.3 is reduced from 43.00 to 3.36 and from 61.78 to 2.01 for loaded and unloaded conditions respectively. Using recommended minimum voltage ratio of 2, L_n=0.02 mH is the maximum critical value of L_n which can be selected for reference for further investigations. Further increase in L_n beyond 0.02 mH looks unrealistic and probably with performance trouble. From design of trap and stack tuners, 0.02 mH is one tenth of the effective inductance of trap circuit and twice the maximum value of design parameter L_n described in chapter 5.

Table 7.1a
Parameters of twin trap for stack tuners in table 7.2b

R_0 ohms	L_1=L_2 mH	R_1=R_2 m-Ω	K	C_h uF	C_l uF	f_0 kHz	SEP Hz	BW Hz
400	0.1	0.1	20	2.531004	2.535057	10	4	15.4

Table 7.1b
Parameters of series/parallel stack tuner for twin trap

No	L_{stack} mH	C_{stack} pF	R_n ohms	L_n mH	C_n uF
1	3618.6	70	9.869604401E-6	1.0E-3	253.3029591
2	3618.6	70	2.4674011E-4	5.0E-3	50.66059
3	3618.6	70	9.869604401E-4	1.0E-2	25.33029591
4	3618.6	70	2.220660990E-3	1.5E-2	16.88686394
5	3618.6	70	3.947841759E-3	2.0E-2	12.66514796
6	3618.6	70	6.168502753E-3	2.5E-2	10.13211836
7	3618.6	70	9.869604401E-2	1.0E-1	2.533029591
8	3618.6	70	3.947841759E-1	2.0E-1	1.266514796

Table 7.2(a)i
Output peaks for diff. L_n values with load on terminals

L_n	Node Names					
mH	BFE	JB1E	LB1E	JB2E	LB2E	JB3E
	Loc1	Loc1	Loc2	Loc2	Loc3	Loc3
				Close	Close	
1E-3	0.0233	0.0547	0.0449	1.275	0.745	0.0305
5E-3	0.114	0.260	0.218	3.35	2.61	0.146
1E-2	0.2227	0.494	0.422	4.303	3.87	0.294
1.5E-2	0.32	0.68	0.61	4.80	4.70	0.44
2E-2	0.425	0.890	0.795	5.283	5.488	0.579
2.5E-2	0.61	1.226	1.126	5.73	6.45	0.856
1.E-1	1.61	2.638	2.780	7.12	8.68	2.572
2.E-1	2.39	3.56	3.08	7.82	9.51	4.46

By expanding output signal voltage from any stack tuner along time scale, not shown here, it is observed that all signals simply contain

10 kHz frequency. Due to concentration of these waves along x-axis, 10 kHz signal output voltages look like completely shaded (due to over lapping of drawing ink) envelopes of beat or burst or packet of waves although they simply contain main fundamental frequency signal of 10 kHz and small percentage of frequencies on both sides of 10 kHz. As shown in figures 7.3 and 7.4, amplitude level, time duration and shape of these envelopes or wave beats for same fault and same fault locator depend mainly upon the individual number of fault locator from the fault and the value of L_n. Since different amplitude level and time duration of beats are achieved by changes in L_n values and number of fault locator, characteristic of beats is not associated with characteristic of type of fault or type of simulation but only upon type of filter, value of its components and number of the individual fault locator from the fault.

Further it looks though best working range of L_n, for high output signal voltage, is between L_n=0.01 mH to 0.02 mH. But for better discrimination of the fault locator signal, all values of L_n lower than 0.01 mH are better in performance. This wide range of parameters allows designer to select best suitable parameters for better performance of the fault locator based upon method of signal discrimination, method of signal processing, type of fault, availability of values of each component in market and series/parallel combination of resistances to realize exact value.

Table 7.2(a)ii
Output peaks for diff. L_n values with load on terminals

L_n	Node Names					
mH	LB3E	JB4E	LB4E	JB5E	LB5E	JB6E
	Loc4	Loc4	Loc5	Loc5	Loc6	Loc6
	Close					
1E-3	0.038	0.0369	0.738	0.0168	0.038	0.03688
5E-3	0.189	0.1835	2.568	0.784	0.1885	0.1834
1E-2	0.375	0.364	3.93	1.448	0.375	0.364
1.5E-2	0.598	0.58	5.00	2.10	0.60	0.56
2E-2	0.739	0.717	5.69	2.49	0.74	0.716
2.5E-2	1.092	1.059	6.71	3.238	1.093	1.059
1.E-1	3.27	3.18	8.88	4.84	3.28	3.18
2.E-1	5.69	5.52	9.6	5.65	5.69	5.52

Table 7.2(b)i

Output peaks for diff. L_n values without load on terminals

L_n	Node Names					
mH	BFE	JB1E	LB1E	JB2E	LB2E	JB3E
	Loc1	Loc1	Loc2	Loc2	Loc3	Loc3
				Close	Close	
1E-3	0.0369	0.0827	0.0719	1.864	1.107	0.0509
5E-3	0.18	0.3965	0.324	4.86	3.906	0.247
1E-2	0.352	0.756	0.6275	6.33	5.88	0.476
1.5E-2	0.515	1.079	0.912	7.13	6.98	0.684
2E-2	0.67	1.378	1.18	7.62	7.70	0.884
2.5E-2	0.956	1.894	1.67	8.18	8.79	1.245
1.E-1	2.42	4.06	4.075	9.94	12.90	2.915
2.E-1	4.08	5.30	5.94	11.41	17.12	4.09

Table 7.2(b)ii

Output peaks for diff. L_n values without load on terminals

L_n	Node Names					
mH	LB3E	JB4E	LB4E	JB5E	LB5E	JB6E
	Loc4	Loc4	Loc5	Loc5	Loc6	Loc6
			Close			
1E-3	0.0675	0.0561	1.112	0.018	0.0675	0.0562
5E-3	0.3295	0.272	3.945	0.87	0.3295	0.272
1E-2	0.641	0.517	5.975	1.68	0.6405	0.517
1.5E-2	0.927	0.755	7.03	2.426	0.932	0.755
2E-2	1.212	0.985	7.57	3.12	1.212	0.985
2.5E-2	1.74	1.415	8.775	4.37	1.74	1.415
1.E-1	4.37	3.74	12.70	10.04	4.37	3.74
2.E-1	6.55	5.77	16.8	13.82	6.54	5.76

Table 7.3(a)

Maximum to minimum voltage ratio of fault locators o/p signal

L_n mH	Fault locator number from source side					
	Loc1	Loc2	Loc3	Loc4	Loc5	Loc6
		Close	Close		Close	
1E-3	2.35	28.40	24.43	1.03	43.93	1.03
5E-3	2.28	15.37	17.88	1.03	3.28	1.03
1E-2	2.22	10.20	13.16	1.03	3.86	1.03
1.5E-2	2.13	7.87	10.68	1.03	3.50	1.03
2E-2	2.10	6.65	9.48	1.03	3.36	1.03
2.5E-2	2.01	5.09	7.54	1.03	2.96	1.03
1E-1	1.64	2.56	3.37	1.03	1.48	1.03
2E-1	1.49	2.54	2.13	1.03	0.99	1.03

Table 7.3(b)

Maximum to minimum voltage ratio of fault locators o/p signal

L_n mH	Fault locator number from source side					
	Close	Close		Close		
	Loc1	Loc2	Loc3	Loc4	Loc5	Loc6
1E-3	2.24	25.90	21.75	1.20	61.78	1.20
5E-3	2.20	15.00	15.80	1.21	4.53	1.21
1E-2	2.15	10.10	12.35	1.24	3.56	1.24
1.5-2	2.10	7.82	10.20	1.23	2.90	1.23
2E-2	2.06	6.46	8.71	1.23	2.43	1.23
2.5-2	1.98	4.90	7.06	1.23	2.01	1.23
1E-1	1.68	2.44	4.43	1.17	1.26	1.17
2E-1	1.30	1.92	4.19	1.14	1.22	1.14

7.2.3 Selection of parameters for fault locator.

By comparison of results from fault locator performance for different sets of parameters in previous section 7.3.2, it was shown that the safe and appropriate working range of parallel stack tuner L_n is between 0.001 mH and 0.02mH in lieu of the 0.01 mH suggested in chapter 5. Fault locator close to fault has high voltage ratio for low value of L_n and vice versa. Best value of L_n for high voltage ratio may be in fraction of micro heneries. However to use fault locator with critical but allowable parameters, L_n=0.02mH is selected for further investigations of the fault locator and reported in the remainder part of this thesis. Suitability of these values will be confirmed in chapter 9 by different methods of application. However for practical application of the fault locator in real network of an 11 kV distribution system much lower value than 0.02mH is of advantage.

7.3 Performance of fault locator having series LCR stack tuner.

In chapter 6, impedance frequency response of the fault locator using both the series LCR and series/parallel stack tuners were determined. These results showed that the series/parallel stack tuners produced expected results of high output from stack tuners close to fault and low output from stack tuners away from the fault. The results for the series LCR stack tuner were doubtful. The results for the series LCR stack tuner using 70 pF gave nearly same output from all stack tuners and therefore it seems that the fault locator using stack tuner capacitance of 70 pF in series LCR will more likely not work. The results for the series LCR stack tuner using 1 pF were, however, acceptable as it produced high output from stack tuners close to fault and low voltage from stack tuners away from the fault. In order to confirm these results and in case 1 pF series LCR is useful, to determine extent of its usefulness, performance of the fault locator with the series LCR stack tuner are determined.

11kV distribution system shown in figure 7.1 has series/parallel LCR stack tuner and twin line trap, the steady state performance of which is already investigated in section 7.3. Replacing series/parallel stack

tuner in figure 7.1 by series LCR stack tuner, consisting of parameters R_0=400Ω, & C_{stack}=1pF correlated with L_{stack}=253.303H or C_{stack}=70pF correlated with L_{stack}=3.8616 H as designed and discussed in chapter 5 for f_0=10 kHz, performance of fault locator with LCR stack tuner is tested. The results obtained are shown in figure 7.5 and 7.6 respectively. These results are obtained from similar EMTP program simulations used in section 7.3.

Results in figure 7.5 are obtained for C_{stack}=1pF. These results show that the fault locator fails to locate the fault as output voltage from the fault locators away from fault is higher than output voltage from fault locator close to fault. Voltage outputs from nodes LB3E, JB4E, JB5E, LB5E and JB6E away from fault are higher in magnitude than voltage output JB2E close to fault. Moreover outputs LB3E and JB4E of Loc4 and outputs LB5E and JB6E of Loc6 are unable to filter the signal properly as output from both sides of the fault locators, as shown in figures 7.5a, and 7.5b, remain nearly the same. This shows that fault locator with series LCR stack tuner having 1 pF capacitance is unable to work properly and is useless for fault localisation. Although in chapter 6, it was computed that the series LCR stack tuner with series capacitance of 1 pF may provide adequate filtration. This wrong prediction is perhaps due to long line length, reflection of waves and some unknown characteristic of series LCR filter circuit. This proves that a fault locator even with a very small value of stack tuner capacitance in series LCR stack tuner is not capable of fault localisation. Thus a simple series LCR stack tuner is unsuitable for all practical purposes as (i) it uses a very high value of inductance (equal to 253.3 H), (ii) output signal voltage is poorly filtered as it contains higher output signal voltage from stack tuner away from fault than output signal voltage from stack tuner close to fault and (iii) over all output signal voltage from stack tuners is very small in magnitude compared to output obtained from series/parallel stack tuners.

Results in figure 7.6 show performance of series LCR circuit using available value of stack tuner capacitance C_{stack}=70 pF. These results once again show that the stack tuner with 70 pF is not capable of separating wanted frequencies from unwanted frequencies. Output from almost all 70 pF stack tuners look of the same magnitude. Output signal voltage JB2E from stack tuner close to fault is less than output signal voltages JB3E,

LB3E, JB4E, LB4E, JB5E, LB5E and JB6E from stack tuners away from fault. Presence of higher output signal voltage from stack tuners away from fault than output signal voltage from stack tuners close to fault confirms that fault locators having series LCR stack tuner is unsuitable for fault localisation. This shows that the fault locator with C_{stack}=70 pF capacitance is useless and unapplicable. For these reasons, fault locators with series LCR stack tuners can not and will not be appreciated for use.

7.4 Effect of fault locator on steady-state performance of the distribution network.

In section 2.5, steady-state behaviour of a distribution network with capacitor banks was selected. Using the same procedure with the selected distribution network but now the fault locators are added at convenient places, as shown in figure 7.7. The steady-state behaviour is simulated for the same nodes JDGA, NA, FA4 and LMA6. Effect of fault locators on steady-state performance of the 11 kV system shows that source voltages are same where as load terminal voltages and currents are slightly less than those found without fault locators (chapter 2). Source currents with fault locators installed in the network are also slightly less than their values without fault locators. However when the two sets of results (with and without fault locators) are drawn on common x-y plane, they look alike, as shown in figure 2.6. The results show that the curves are sinusoidal and steady-state in waveforms. When terminal voltages at nodes FA4 and LMA6 are compared, they look nearly the same due to (i) the same power line length (ii) the same number of fault locators between source and load terminals and (iii) the same type of load in both cases. Comparing load voltages and currents at NA with FA4 (or LMA6), it is found that higher voltage drop takes place in FA4 (or LMA6) due to the length of line, although load currents in FA4 are smaller than NA. Comparison of peak values of corresponding currents and voltages at these four nodes with and without fault locators shows that the line impedance has increased after installation of fault locators. The effect of increase in impedance has caused a slight decrease in line currents and terminal voltages. Maximum decrease in present case in currents and terminal voltages is in between 0.0% to 1.7% depending upon type of variable and

location of measurement.

7.5 Effect of fault locator on transient behaviour of the network

In section 2.6, transient behaviour of the distribution network with capacitor banks was studied for a solid earth fault at YARB. Using the same procedure and the same distribution network, but now with fault locators inserted at convenient places, effect of fault locator on transient behaviour of the network is simulated for same nodes. Complete circuit arrangement of the network is shown in figure 7.7, in which high value resistance between earth and YARB are replaced by a low resistance of 0.000001 ohms. The transient results when drawn with the results without fault locator in figure 2.8, the two look identical, due to the large scale used for current and voltage along y-axis. Although transient results of both cases with and without fault locator for the same 11kV system look the same on paper, they are, in fact, not exactly the same in magnitude as already confirmed by the steady state values. Careful study of peak values of transient current and voltage in both cases reveal that the peak transient values in distribution network with fault locators are smaller than the corresponding values without fault locators. The maximum variation observed is 1.876%. Similarity in shape confirms that effect on transients due to the inclusion of fault locators is small and therefore there should be no cause of concern for accuracy of results. The shape of currents and voltages follow general pattern and rules of a fault in a distribution system, as described in section 2.6.

7.6 Conclusions

In this chapter, careful testing of fault locator for the designed parameters is carried out utilising EMTP simulation with 4.5 micro seconds step size. More than 30 simulations, using different parameters were executed. Each simulation took nearly 8 hours to complete using a PC 25 MHz. Selected important results are shown in tabulation and graphical form. Time consuming tests reveal the following conclusions:-

1. Wave shape and amplitude of output waves from stack tuners change with change in L_n, although fault location, circuit configuration,

source voltages and transient currents and voltages remain the same. Higher the value of L_n, higher is the magnitude of voltage signal from each stack tuner and the output beat contains smaller duration and bigger amplitude. Since transients are same in all cases, characteristics of variation of size and magnitude of beats of output signal voltage is the characteristic of filter and magnitude of its parameters only.

2. Output voltage from any stack tuner using either series LCR or series/parallel stack tuner, when expanded along x-axis in time scale, shows only 10 kHz signal wave form.
3. Fault locator using series stack tuner has totally failed to give discriminative output signal voltage and therefore may never be tried in future for any application in power systems.
4. Fault locator using series/parallel stack tuner, at low value of L_n. (or low bandwidth) give very successful discriminative output signal and therefore could be used for any application in power systems.
5. Ability of fault locator using series/parallel stack tuner for fault localisation is inversely proportional to value of L_n (i.e. bandwidth of the filter for a constant resonant frequency f_0 is proportional to L_n).
6. For proper testing of fault locator, a practical situation of fault and travelling waves should always be used. Transients without load are higher than with load. Transients in longer power lines may by-pass small amount of resonant and related frequencies through stray coupling to other side of trap circuit. Reflection and scattering of waves can be expected in tapped lines, due to mismatching of surge impedance of lines at locations of line tapping. However for a fault locator properly designed, as in present case, the operation of fault locator should not suffer by any means either by length of line or by tapping of lines.

Chapter 8

REMEDIES TO CAPACITOR BANK BY-PASSING EFFECT

8.1 Introduction

In chapter 7, simulation of fault transients of a 3-phase distribution network was carried out without capacitor bank, with the assumption that it would avoid by-passing of high frequency transient waves through capacitor banks to earth, which otherwise could create trouble for a closeby fault locator in not allowing these frequencies to reach its stack tuner. Capacitor banks are very widely used for voltage regulation of distribution systems. Use of these has to continue as usual with and without fault locators.

8.2 Effect of capacitor bank on performance of fault locator.

Figure 8.1 shows the distribution network of figure 7.1 with capacitor banks at FA2, FB2, and FC2 to investigate the effect of capacitor bank on performance of the fault locator. Using solid earth fault, as in chapter 7, performance of fault locators Loc2 and Loc3 close to fault and close to capacitor banks as shown in figure 8.1, is studied. Figure 8.2 shows that only one 3-phase stack tuner on the left side of the fault (i.e. away from capacitor banks but close to the fault on the source side) detected the occupance of the fault. This must be compared with the fault detection illustrated in chapter 7 for the case without the capacitor banks. This proves that due to presence of capacitor banks at F*2, Loc3 and Loc5 are unable to receive fault waves to detect the fault. This evidently shows that performance of the fault locator has now suffered from the shunt capacitor bank.

8.3 Proposed remedies

One of following three solutions can be applied to stop the

flow of high frequency waves through the capacitor bank which affected the performance of the fault locator.

i) Use of capacitor banks at load terminals (power factor correction) in lieu of the present shunt capacitor

ii) Insertion of trap circuit in series with capacitor bank

iv) Installation of capacitor bank in middle of trap of fault locator

Each of the above will now be investigated.

8.3.1 Use of power factor capacitors at the load terminals in lieu of the shunt capacitor

Figure 8.3 shows new arrangement of capacitor bank for 11kV distribution system. These capacitors are now located at N*, LM*6, & F*4 close to individual loads. Value of capacitance is determined by equ. 2.6. Performance of fault locator under new capacitor bank arrangement for fault locators Loc2 and Loc3 is shown in figure 8.4. The results show that all fault locators are now working perfectly as expected. Fault location is distinctive due to the high difference in output voltages from stack tuners closest to fault while low output voltages from rest of stack tuners away from fault. This proves that the new arrangement is quite successful and effective both for (i) p.f. improvement and (ii) accurate fault localisation. This method should be encouraged in simple radial system where tapping and interconnection of power lines are not in use.

8.3.2 Insertion of trap circuit in series with capacitor bank

Figure 8.5 shows the same arrangement of figure 8.1 but with trap circuit inserted in series with capacitor banks. In this arrangement same line trap, as used in fault locator, is used in series with the capacitor bank. This trap produces high impedance to resonant frequency f_0 and frequencies around resonant frequency f_0 and therefore these frequencies can not flow through the capacitor bank. For resonant and surrounding frequencies, this trap circuit acts as a switch in its off position and passing of these frequency waves through the capacitor bank become impossible. As impedance of the trap circuit at 50 Hz is low, performance of capacitor bank is not affected. The results obtained by this arrangement for fault locators Loc2, Loc3 and Loc5 are shown in figure

8.6. The results show that all fault locators close to the fault are capable of giving high output voltage together with high voltage ratio and therefore the by-passing of high frequency transients through capacitor banks is stopped.

8.3.3 Installation of capacitor bank in middle of trap of fault locator

Figure 8.7 shows new arrangement of fault locator in which one extra 3-phase fault locator is installed at F*2, and tapped line as well as capacitor bank are installed at middle of the new installed fault locator. This new arrangement allows the same length of power line with the same relative positions of the remaining configuration of the power system. This method is very effective in preventing flow of high frequency waves through capacitor bank provided fault locator can handle connection for capacitor bank and power line if and when required. This method also provides safe guard against reflections and scattering of travelling waves caused by mismatch of surge impedance at tap junction. Simulated results for fault locator Loc2 and Loc7 for solid earth fault at YARB is shown in figure 8.8. The results show that fault locators Loc2 & Loc7 have localised the fault in the expected position (YARB). Since fault localisation is done by only two adjacent fault locators, the fault localisation by this method is more precise and much improved than by any other method. High fault localising voltage outputs are obtained only from two stack tuners, one on each side and close to fault. Difference in high output voltage levels from stack tuners close to fault and low output voltage signals from rest of stack tuners easily and conveniently localises the fault. This method is very much effective in multiple shunt capacitor compensation. In such system, each capacitor bank is connected at the middle of extra fault locator.

8.4 Comparison of methods for stopping high frequency waves flow through shunt capacitor banks

Comparison of results of all the three methods show that the last method number 3 (i.e. installation of capacitor bank in the middle of trap of fault locator) is the best, as it has (i) high output signal voltage level of stack tuner on source side of fault locator Loc2 close to fault

as well as stack tuner on load side fault locator Loc7 close to fault, (ii) higher voltage ratio of load side fault locator Loc7 close to fault than those from other methods as shown in figure 8.8b and (iii) negligible output signal voltage (not shown here) from all fault locators on load side away from fault. This method has other advantages as described in section 8.3.3.

Chapter 9

APPLICATION OF THE FAULT LOCATOR
(Using the fault locator for universal fault localisation)

9.1 Introduction

In this chapter, different methods of application of the fault locator which were designed and tested in previous chapters are investigated for fault localisation in the selected distribution network. This is to highlight relative merits and usefulness of each method of application.

9.2 The principal differences of fault location system to fault protection system

In standard practice, protection of distribution system against damage is a function of circuit interruptors. The circuit breaker protects the system by opening its terminals to separate faulty section from remaining healthy ones. Terminals of the circuit breaker are opened by energising circuit breaker coil connected to a relay and a remote control sensor available on the circuit breaker. To energise the circuit breaker coil, the relay is energised by one of several methods using one of the fault measurands of the power distribution system. Different types of relays working on different measurands are necessary to protect the power system against different faults under different requirements of discriminative configuration, operating conditions and constructional features of the power system. Each type of relay usually responds only to preset magnitude of any one of various functions or measurands of the power system quantities namely the voltage and current. When the threshold value of a relay is met, the relay closes a contact which in turn energises the circuit breaker coil which separates faulty section from healthy system.

In standard practice, fault localisation of distribution system should be a function of an alarm. Before the alarm is triggered, its operating coil must be energised, and this, in turn, requires that certain

comparator (or relay) will also be energised by the fault locator, in a similar way as used in protection system. The main difference between the protection system and the fault location system is that in the protection system all fault related circuit breakers are organised to operate in a backup feature, according to the priority for separating the faulty section. This is to ensure that minimum number of consumers are affected. While in the fault location system, only the alarms corresponding to fault locators close to and on both sides of the fault are allowed to operate. Thus in protection system any one of the circuit breakers on same protection schemes must operate to save the system and therefore more than one circuit breakers and backup relays are used. But in fault localisation system, emphasis is on precise localisation and therefore only alarms which are directly related to the fault locators on each side and close to the fault must operate. Thus for determination of exact location of fault, a fault localisation system can not use a backup system exactly in the way it is used by the protection system but on the contrary the fault location system takes all necessary steps to avoid other fault alarms related to fault locators away from the fault not to operate.

Use of same f_0 in all fault locators of the present fault localisation system ensures that only the fault locators on both sides and close to the fault will operate. The fault location system has to send a clear message about precise location of the fault after it has taken place, contrary to the protection system where tripping of the circuit breaker close to the fault is not necessary, though it is preferable.

As shown in previous chapters, as soon as a fault occurs, signal fault voltages of different magnitude start appearing in all stack tuners. Initially the fault signals are in nano and micro volts which appear right from the fault inception moment. Later these become of some significance in magnitude in the range of millivolts and then increase rapidly in magnitude in the range of millivolts and volts, depending upon location of stack tuner, type of fault, circuit configuration etc. For fault localisation, mere availability of fault signal in an stack tuner is not enough to operate a fault alarm. The fault measurand has to be separated from the power network and compared with a reference value through a relay or comparator. The reference value and its type of relay, like in fault protection system, would depend upon type of fault, configuration of the

11 kV distribution system at the time of fault and above all the method of application of the fault locator. Like protection system, the different reference values for comparators in fault localisation can easily be provided by conventional relays, comparators or signal processors. The relay, or comparator or signal processor when receives the fault signal exceeding the reference magnitude, then it interprets the input fault signal properly by energising a contactor of reliable voltage source which again energises the corresponding fault alarm. The alarms are usually installed close to service staff on duty so that when an alarm rings, the service staff on the duty can clearly understand the message of fault and respond to it accordingly.

Signal processing and interpretation of the fault signal voltage can be carried out either at fault locator site locally and then the resulting message or the filtered fault signal is sent to appropriate authority at the central station for processing and interpretation by suitable equipments or personnel. Thus a proper and precise fault location system, like a proper protection system, requires some communication link between comparator or relay and the alarm as well as other devices. Compared to signal processing at the central station, the local signal processing seems to have more advantages than the signal processing at the central station as it avoids fading of fault signals by radio frequency radiation into surrounding atmosphere and conductors, induction of noise from conductor joints or cracks into the signal, deterioration of signals by interference from close by broadcasting stations etc. Also local signal processing adds in simplification in installation of equipments and servicing (without interruption into other functions at central station). Local processing system will also easily operate local fault alarms and fault display panels before sending the fault message to the central station.

Thus local signal processing requires less effort, introduces less error, produces superior result and achieves better use and performance than the signal processing at the central station. If the signals are processed at the central station away from the fault, modal combination of the fault signals which would be received at the central station, becomes a complete necessity [1,3,5]. Finally if the fault signals are low in magnitude they can be amplified and processed locally at each fault

locator before loosing them in transmission links. Alternately the output voltages which are low can be used to operate a relay instead of the fault alarm, like in protection systems, and then the relay signal can be allowed to do different kinds of works including operation of the fault alarms. Signals which are very low in magnitude to operate a relay or a comparator, may be amplified before operating the relay or comparator.

9.3 Methods of application of the fault locator for fault localisation

Fault locator arrangement of the 11 kV distribution system of figure 8.7 is used to investigate methods of application of the fault locator in this chapter for fault localisation. For convenience these methods of investigations are named as below :-

i) 1-phase type
ii) modal type
iii) 1-phase rectified type
iv) modal rectified type
v) 1-phase integrator type
vi) modal integrator type
vii) modal raised integrator type
viii) source-side multi-frequency output type
ix) universal fault localisation type

All these methods are investigated in the coming sections.

9.3.i 1-phase type application to the fault locator

The principle of the circuit arrangement for this type of application is shown in figure 9.1a. This circuit arrangement is the same as that shown in figure 8.7 but due to lack of space, it shows only two fault locators Loc2 and Loc7. Fault signal voltage is extracted by a parallel resonant circuit via magnetic coupling from the parallel resonant circuit of the stack tuner. Circuit components of the two parallel resonant circuits are exactly the same to get maximum output filtration at 10 kHz. Designing of two magnetic coils is assumed to have radio frequency magnetic core with maximum coupling. The extracted fault signal is fed into an ac relay shown in figure 9.1a, which has two parallel coils

fed from single source. The two coil split arrangement is normally used to avoid vibration of the armature during zero crossing of a.c. signal [44]. Due to the high resonant frequency f_0 of the fault signal, the vibration may have very little effect on the performance of the armature at zero crossings with or without the two coil arrangement. Using digital simulation, output fault signals, obtained for 1:1 transformation ratio of the magnetic coupling from all stack tuners are shown in figure 9.1b. Threshold level for operation of the relay is 3.5 volts. These figures show that only two stack tuner outputs JB2E and T1BFE of Loc2 and Loc7 respectively, one from each side of the solid earth fault at YARB on phase B, give higher voltages than the threshold 3.5 volts. These signals belong to Loc2 and Loc7 and operate their corresponding a.c. relays as soon as the fault signals cross the threshold level of 3.5 volts. These relays in turn energise fault alarms representing and bearing name plate of names Loc2 and Loc7. At and above threshold voltage of 3.5 V the armature would be attracted by flux in the main core of the relay, and a lever attached permanently to the armature moves with the armature movement and pushes a switch to the ON position. The ON position of the switch closes a dc circuit energising local as well as central station fault alarms, precisely indicating exact location of the fault. The switch and the lever positions are such that the lever can only turn the switch to ON position and not vice versa. To set the switch to OFF position, it requires manual adjustment. Operation of the fault alarms representing Loc2 and Loc7 at the central station declare loudly by their ringing sounds that "these fault locators have found a fault in the distribution lines". The service staff hearing the sound check individual name of the fault locator on the loud sounding fault alarms. Thus they become fully aware of the fault locators responsible for setting them into the ringing position. They then rush to the distribution system between the corresponding fault locators. Reaching at the site between Loc2 & Loc7, the service men check the faulty conductors and clearly carry out the required service. Thus the fault is localised. As fault in this case is solid earth fault and that it is a serious one, a circuit breaker will isolate the faulty section well before the arrival of the service staff at the fault site.

In this type of application of the fault locator, sensitivity of the relay or comparator needs careful adjustment for detecting faults.

Figure 9.1c shows fault locator signal outputs for a ground fault on line B through a high impedance of 1000 ohms resistance at YARB. To detect this fault the threshold level is reduced from 3.5 volt to 1.0 volt. With this assumed new relay setting of 1.0 volt, for the case of a solid line to earth fault, the relay will detect the fault at least at 6 locations (see figures 9.1b). Thus fault localisation by new low level relay setting threshold level of 1 volt, while it detects all range of faults between 1000 ohms to 0 ohm line to line, line to ground faults, now the new threshold level of 1 volt operated 6 relays instead of 2 which is erroneous. Ringing of 6 fault alarms produces confusion in fault localisation.

This proves that this type of application of the fault locator is not suitable for fault location. Another disadvantage of this type of application is that this type of application of the fault locator will have little distinction between arcing and nonarcing type faults. In this type of application fault localisation in arcing and non arcing faults depends only upon maximum peak value of the fault signal. Third draw back of this type of application is that it is one of the applications using maximum number of relays, alarms, switches, signal carrying conductors etc, number of each device being used is equal to the number of 1-phase fault locators.

9.3.ii Modal type application to the fault locator

Figure 9.2a shows the summation of the three phase outputs with the appropriate ratios to achieve the modal ac type application of the fault locator for a fault between locators Loc2 and Loc7. For lack of space, the 3rd set of the stack tuners of Loc7 is not shown. This type of application of the fault locator is similar in operation to the previous application of the fault locator described in section 9.3i except that modal voltages instead of 1-phase voltages are used in the present case. The sequence of events for the operation of the relay/switch, fault alarm, their picking up and resetting, comparison of fault signal with threshold level, decision making for fault location etc, are the same as described in the previous section 9.3i. For this reason the conclusion on the advantages and disadvantages is the same. The difference between the two is that the

modal voltages are higher as shown in figure 9.2b. This is for solid earth faults and figure 9.2c for line to earth fault but through 1000 ohms fault resistance. From the output signal strength and threshold level of 3 volts shown in figures 9.2b signal discrimination between the fault signals and threshold level is high and reliable in present case.

Modal signal output voltages in figure 9.2b from fault locators Loc2 and Loc7 are about 15 volts compared to threshold level of only 3 volts and therefore this method of application of the fault locator localises the fault accurately. Figure 9.2c shows modal voltages for line B to earth fault through 1000 ohms resistance at YARB. The new threshold level is 1.0 volts. With this new low level threshold setting, a solid earth fault, as shown in figure 9.2b resulted in maloperations of 4 fault locators. This proves that this system can not be used for fault location.

Note that figure 9.2a shows successful modal [1,3,5] mixing of the 3-phase of the 1-phase voltage scheme through magnetic coupling. With the TACS, signal processing has been used in this application to transform the 3-phase fault signals after 1-phase fault locator system into the single mode of Karrenbauer transformation. This modal combination of 1-phase fault signals in the ratio of (1,-2,1) do not only increase the resulting modal signal output level directly from a 3-phase fault locator system, but it also ensures that all common disturbances are removed. The common disturbances include striking of broadcasting signals, outer atmospheric radiation, cloud charging, voltage induction from neighbourhood communication and power lines etc. This combination is particularly useful when distance between fault location and processing units is considerable compared to wavelength of the resonant frequency f_0. Transmission of high frequency fault signal by overhead lines is actually transmission of radio waves by lines which not only captures the noise but also dissipates energy by propagation into the atmosphere. This transmission of 10 k Hz signal represents the two most above mentioned common problems of the radio waves which influence quality of the fault signal received at the far end for the signal processing.

9.3.iii 1-phase rectified type application to the fault locator

Figure 9.3a shows circuit arrangement for 1-phase rectified type

application of the fault locator. In this type of application of the fault locator, ac fault signal extracted from the per phase stack tuner is rectified before applying to the relay. The rectified output voltage from each per phase stack tuner is shown in figure 9.3b. Each rectified signal, like its original unrectified signal shown in figure 9.1b, look dark in its envelope due to closely drawn lines presenting variable nature of the instantaneous values of the rectified signals. The darkness of the signal shows that the instantaneous values vary almost from 0 to peak values. Curve No.9 in figure 9.3b shows expanded shape of the rectified signal in curve No.8 (ABL7). In order to reduce possible armature fluctuations, the rectified signal may require either use of an ac type relay or smoothing of the rectified signals by dc pass filter circuit (not shown here). The performance results and general working principle of this type of application of the fault locator remains similar to the previous application of the fault locator covered in section 9.3i. Even with smoothed dc, no further improvement is expected except when the smoothed dc is used by static relays, electronic comparators and electronic switches. As this circuit uses rectifiers in addition to all other conventional devices of the previous application (see section 9.3i) for almost the same performance, this application is not suited for the fault location. This application suffers from the same disadvantages explained in section 9.3i and 9.3ii relating to the low and high resistance faults.

Another method of using 1-phase rectified signal is by comparing the rectified signals from the two sides of the same fault locator per phase. This method was tried, the results remained the same with the same level problems. For no new information and presence of maloperation of relays in addition to other disadvantages and use of extra devices, this method is not suitable for fault localisation.

9.3.iv Modal rectified type application to the fault locator

This method of application to the fault locator is similar to 1-phase rectified type application discussed in section 9.3iii. The modal voltages instead of 1-phase voltages are used. When this method was tried, it gave identical results and suffers from the same disadvantages as explained in sections 9.3i,9.3ii & 9.3iii. For these reasons this method

is not suitable for fault location. The circuit arrangement of this method is shown in figure 9.4a. The resulting modal rectified output voltages for solid earth fault are shown in figures 9.4b.

9.3.v 1-phase integrator type application to the fault locator

a. The principle

Figure 9.5a shows circuit arrangement of the 1-phase integrator type application of the fault locator. Method of signal extraction and rectification used in this application is the same as used in sections 9.3i and 9.3iii, and in fact the 1-phase with the rectified voltages are the same as shown in figures 9.1b and 9.3b respectively. After rectification, the signal is integrated with time. Rectification of the fault signal before integration is compulsory to avoid subtraction of the signal by negative integration. For integration of the rectified fault signals, RC integrator circuit[43] can not be used, as the integrator circuit works on the principle of simultaneous charging and discharging of signal voltages, as explained in the following section 9.3vb. For this reason, signal processing method is the only available method for this type of application. This method uses full facility of signal processing for every process after signal extraction from the stack tuner up to operation of the fault alarm. For successful operation, additional operations such as automatic readjustment of the integrator to zero is required by the signal processing. The integrator output signals obtained from EMTP are shown in figure 9.5b. The threshold level is 35 milli volts-sec. Compared with the threshold level of 35 milli-volts-sec adapted in this case, only two fault signals, IL2 from Loc2 and IR7 from Loc7, one from each side and close to the fault (at YARB) are capable of operating their corresponding relays or comparators or signal processors. Alarms and display panels are energised by signal processing after receiving signals from Loc2 and Loc7. The maintenance now will take up the findings and carry on the sequence of repair.

Figure 9.5c shows 1-phase integrated voltages for line to ground fault through 1000 ohms at YARB. The figure shows signals for this high shunt fault resistance. They are lower than the corresponding solid line

to earth fault signals. For this reason a low threshold value of 10 milli-volt-sec is used for the new case of the fault location. However with this new setting of the relay or comparator, if the same solid earth fault occurs then the output voltages shown in figure 9.5b, would maloperate at least 4 more fault locators. For this maloperation of the 4 more relays, this method of fault localisation can not be used.

In present example dc energy source is shown to communicate fault messages from local signal processing at individual fault locator through separate control cable links to the primary station but for longer distances other communication means such as radio link, satellite communication, carrier system or public telephone can be used to send automatic fault messages to the service staff at the primary or the central station (load centre).

Another method of using 1-phase integrated signals is mutual comparison of integrated signals from two sides of each fault locator. In this type of application the integrated signals from two sides of each fault locator are compared to find level of difference of the integrated fault signals. This method of application was tested. It was found that the signal difference was positive for some fault locators and negative for others. Extra signal processing steps are required to compare these positive and negative values into meaningful results. Using integrated signal differences it was found that the resulting information is the same. This method also suffers from the same disadvantages discussed in sections 9.3i to 9.3iv and mal-operation of relays. Due to extra effort for same information and other disadvantages, this method of application of the fault locator can not be used.

b Unsuitability of RC integrator circuit in fault location

Figure 9.5d shows an RC integrator circuit used in TV and computer circuits [43], where input voltage signal is usually a rectangular pulse of pulse duration T_p. From this circuit we have

$$v_1 = i R + \frac{1}{C} \int i.\, dt \quad \text{----} \qquad (9.1)$$

$$v_2 = \frac{1}{C}\int i.\,dt \quad \text{-------} \qquad (9.2)$$

If $R >> X_C$, equation 9.1 becomes

$$v_1 = i\ R \quad \text{----------} \qquad (9.3)$$

Putting i from equation 9.3 into equation 9.2, equation 9.4 is obtained

$$v_2 = \frac{1}{CR}\int v_1 .\,dt \quad \text{------} \qquad (9.4)$$

Equation 9.4 shows that the output is faithful integration of the input voltage v_1. Equation 9.4, also shows that the output voltage v_2 is inversely proportional to time constant CR of the RC integrator circuit. Curves d and e in figure 9.5d show effect of time constant CR on output waveform.

Derivation of above equations is based upon the assumption that the capacitor has no previous voltage across its plates and that the applied voltage is of constant magnitude over pulse period T_p. If the capacitor is already charged to a voltage value v_0, then the output voltage equation suggested by reference [43] is as given in equation 9.5

$$v_2 = v_1(1- e^{-t/CR}) + v_0\ e^{-t/CR} \quad \text{-------(9.5)}$$

where v_0 is the instantaneous residual voltage, across the capacitor, at the time when v_1 is applied to the integrator circuit. In equation 9.5, first part represents charging of the capacitor and the second part represents discharging of it. If the signal v_1 is variable and the capacitor is continuously holding a continuous variable voltage across its terminals, then equation 9.5 is applicable for each movement. In this situation the instantaneously varying applied voltage v_1 charges the capacitor and the instantaneous existing voltage on the capacitor discharges the capacitor. If v_0 is higher than v_1, the capacitor discharges at a rate higher than the rate of charging. Since the fault rectified signals are variable between zero and peak values, in this case, the capacitor will have in average zero voltage across its terminals. This confirms that this integrator circuit can not be used for the integration

process in fault localisation system.

9.3.vi Modal integrator type application to the fault locator

The principle of the modal integrator type application of the fault locator is similar to the 1-phase integrator type. The difference between the two is that the modal integrator type application of the fault locator uses modal voltages instead of suggested 1-phase voltages. The circuit arrangement using this method is shown in figure 9.6a where as the signal outputs and the threshold voltage are shown in figure 9.6b. This method is tried and from the results it is found that this method of application suffers from the same fault resistance disadvantages as described in section 9.3v for 1-phase integrator output. For these reasons this method can not be used either.

9.3.vii Modal raised integrator type application of the fault locator

This method was previously used by El-Hami, Johns and Daruvala [1,3,4,6] in fault location using techniques of signal processing. The same authors explained this process of fault location by comparing modal integrated voltages from two sides of each fault locator. They raised the modal voltage to the power of 2 and then integrating the resulting signal. In their case they compared the integrator raised voltage of two sides of each fault locator. They called this method of fault location, as energy level detection technique. In their case, they used signal processing from filtration of the signals to the decision making.

In this section, fault localisation by modal raised integration type application of the fault locator is investigated by signal processing alone. Figure 9.7a shows the basic circuit arrangement for modal raised integrator type application for the fault locator. In this method, signal extraction and modal transformation is carried out as explained in previous sections. Then the modal voltage is first raised mathematically to the power r (where r is even and greater than 0) by signal processing to enhance the modal signal and then finally the raised voltage signals are integrated by signal processing methods. Squaring the modal signal and its integration is in fact done in this method in which r=2 is used.

Squaring of the modal components converts negative half cycles of the components into positive quantities so that integration by signal processing becomes positive and increases with the increase in time. This method in operation is similar to modal integration method investigated in previous section where the modal signals were first rectified and then integrated. Purpose of rectification or raising of voltages to a higher even order is the same, i.e. to obtain positive quantities for integration. However by squaring the modal voltages, it boosts those signals which are higher than 1 volt and reduces all those signals which are fractional below 1 volt. In this type of application of the fault locator, only two cases (i) r=2 and (ii) r=10 are considered. The signal outputs from fault locators close to fault for r=10 are much higher and better than their corresponding signal outputs for r=2. Higher value of r has advantage of causing collapse in low modal signals to near 0 value.

Figure 9.7b shows modal raised integrated signals for r=2 for solid earth fault at YARB. The threshold level is 50 milli volt^2-sec. For this threshold level, only two outputs IMR2 from Loc2 and IML7 from Loc7 are capable of operating the relays. Figure 9.7c shows modal raised integrated signals for r=2 for line to ground fault through 1000 ohms fault resistance. In this situation, the threshold value can be any value between 20 to 150 milli-volt^2-sec. If threshold value of 20 milli-v^2-sec is selected, then in the event of a solid earth fault at least two more relays operating on signals IMR1 and IML2, as shown in figure 9.7b will also operate. Operation of these relays provide wrong messages. For successful operation this method needs careful selection of threshold level. However success of this method depends upon success of selecting threshold level.

Now consider the case for r=10. The circuit arrangement for this application is the same as shown in figure 9.7a. In the present situation of r=10, the modal integrated signal voltages from stack tuners close to fault, as shown in figure 9.7d, has increased to about 1500 Mega units (1 unit = 1 volt^{10}-sec) whereas output signal voltages from stack tuners away from the fault has become so small that EMTP could not print a graph out of signals IML3, IMR3 from Loc3, IML4, IMR4 from Loc4, IML5, IMR5 from Loc5, IML6, IMR6 from Loc6 and IMR7 from Loc7. Signals IML1 and IMR1 from

Loc1 and IML2 from Loc2 away from fault are also negligible compared to 1500 Mega units and therefore appear zero on the zero-line when these are drawn on the same scale. In order to show magnitudes of IML1, IMR1 and IML2 they are redrawn in figure 9.7e on expanded scale. Confirmed from figure 9.7d, the threshold level for signals in the figure is just 1 unit of the integrated signal after being raised to power 10. The modal raised signal ratio (high value divided by low value) for the signal outputs from two sides of the fault locator (Loc7) is now infinite where as this ratio for Loc2 is about 15000 Mega. This high signal ratio of Loc2 and Loc7 with their very high output integrated signals is a complete success which has been achieved in fault location by this method. This success is due to the fact that a fractional quantity raised to a high value becomes very small and vice versa. This is further confirmed from similar results, shown in figure 9.7f, for line to earth fault through 1000 ohms fault resistance at YARB. In figure 9.7f, IMR2 from Loc2 and IML7 from Loc7 are 520 & 550 volt^{10}-sec respectively. Figure 9.7f shows that threshold level of 1 unit is still valid. Contrary to previous methods this method does not require careful selection of the threshold level. This method of application does not suffer from malopration of the relays. As 1000 ohms shunt fault resistance is equivalent to low level arc faults and discharges, these results show that by this method all low level arc faults, high resistance faults and discharges can be detected. This confirms that this method does not suffer from mal-operation of relays.

9.3.viii Source-side multi-frequency output type application
(Remote output type application)

a. Twin trap version

Up till now fault location has been through local stack tuner closest to fault. As the output signals are high frequency signals and away from service staff, extracted signals need extra equipments to (i) boosting signals from fading and (ii) communicate the output signal message from each fault locator to the service station. In order to avoid both of these problems, it is necessary to serve fault location by some means at service station. This is achieved by multifrequency application of the fault locator, whereby each fault locator and corresponding stack

tuners use different centre frequency. In this section, this principle will be investigated.

Figure 9.8a shows phase B circuit arrangement for remote multi-frequency output type application. Six fault locators Loc1-Loc6, each with a twin trap designed at different frequency, are used in the 3-phase 11 kV network system. Output is collected from across parallel branch of stack tuners. For this application a set of six stack tuners, each one resonating to different single centre frequency, is connected with each node JDAF, JDBF, and JDCF at source side which is service station either primary or central station. For convenience the nodes from which outputs are obtained are named JA1E, JB1E, JC1E for Loc1, JA2E, JB2E, JC2E for Loc2 and etc.No output is obtained from any stack tuner on either side of Loc1 to Loc6. In fact to facilitate easy access to output signals, bus bars from JDAF, JDBF and JDCF are extended into a service room, where all 18 stack tuners are connected to these extended terminals. These stack tuners are enclosed in a close box, with their indicating accessories enclosed into a glass window and fault alarms (if any) in the same glass. As soon as line to earth fault at YARB for instance (between Loc2 and Loc3) takes place, high noise frequencies are generated at fault point. These frequencies travel in all directions along lines, away from the fault. These frequencies, while travelling to JDAF, JDBF and JDCF (i.e. location of filtering and using different noise frequencies), cross Loc1 and Loc2. Trap circuit of Loc1 and Loc2 are designed with centre frequencies f_1=10kHz and f_2=15kHz respectively. Consequently trap of Loc1 blocks f_1 and its surrounding frequencies and trap of Loc2 blocks f_2 and its surrounding frequencies. When travelling waves reach JDAF, JDBF and JDCF, frequencies f_1 and f_2 along with narrow band of frequencies on each side of f_1 and f_2 would be missing due to their blocking by line traps of Loc1 and Loc2 respectively. Consequently outputs from stack tuners of the source will show negligible of outputs at these frequencies, as shown in figure 9.8b for per phase output voltages and figure 9.8c for modal phase combination. These modal output signal voltages show that less than 0.35 volts are obtained form signals of stack tuners resonated at 10kHz and 15kHz for Loc1 and Loc2 respectively. For this case, these outputs when compared with outputs from other stack tuners resonated at f_3 to f_6 corresponding to Loc3-Loc6 are less than one sixth. Presence of high

outputs from stack tuners for Loc3-Loc6 shows that these frequencies are not attenuated for obvious reason and this is the absence of these fault locators Loc3-Loc6 between fault location YARB and JD*F. If threshold level for operating alarms etc is above 0.5 volts, fault alarms corresponding to Loc3-Loc6 will operate while those for Loc1 and Loc2 will not operate. This confirms aforementioned principle of detection.

Low outputs from 10kHz and 15kHz stack tuners for Loc1 and Loc2 respectively shows that the fault location is beyond Loc1 and Loc2 as seen at the service station. Presence of high outputs from 20kHz, 25kHz, 30kHz and 35kHz stack tuners for Loc3-Loc6 show the fault location is before these fault locators as seen from the service station. Combining the data, the fault is between Loc2 and Loc3. With this information, the service staff is dispatched directly to the line section between Loc2 and Loc3, where they check the faulty conductors and carry out necessary repair work.

Output from this application has the disadvantage of having inconsistent output for unknown reasons. The most likely reason or reasons may be (i) high impedance of trap circuits interfering performance with one-another, (ii) creation of extra low magnitude resonant impedances arising from the vicinity of $f_1..f_6$ circuits, (iii) shifting of centre frequencies $f_1..f_6$ of the fault locator traps from the centre frequencies of corresponding stack tuners and (iv) diversion of centre frequencies of traps designed for blocking high-frequencies to capacitor bank. Whatever the cause or causes, the output signal at the primary station is not affected much to stop its performance in this type of application. This is confirmed by using different frequencies for f_1 to f_6 in each case. Each time for the same fault, it is found that outputs for Loc3-Loc6 are higher than the outputs from Loc1-Loc2. However, in each case, relative magnitude of outputs from Loc3 to Loc6 varies.

This system has another disadvantage and that is having shorter duration of transient frequencies. This duration improves (increases) with disconnection of the regulating capacitor banks and their associated trap circuits. The reason for this behaviour is not easy to explain and requires further investigation.

b. Two-branch trap version

Figure 9.9a shows similar arrangement as shown in figure 9.8a. This circuit arrangement is obtained by replacing twin traps by two-branch traps (for definition, design and characteristics see chapter 4). A two-branch trap is a simple basic trap circuit whose parameters can easily be designed, modified and compared to other types of traps. Parameters of each stack tuner, trap circuit and consequently corresponding fault locator are redesigned with much lower value of power coil inductance for trap circuit and that of parallel branch of the stack tuner, as shown in table 9.1. The table shows the designed parameters for the 6 fault locators of the circuit arrangement given in figure 9.8a and 9.9a at same place for comparison purpose. These values when compared that the power coil in two-branch traps uses exactly one fourth value of the inductance used in twin trap. Yet the performance with two-branch traps is proved to be slightly better than that with twin traps. This is possible by selecting new lower values of L_n of parallel branch of stack tuners, as explained in chapter 5. The performance output of fault locator in circuit arrangement of figure 9.9a is shown in figures 9.9b and 9.9c. These outputs once again confirm previous results. Similar to previous case outputs from both Loc1 and Loc2 are smaller than those obtained from Loc3 to Loc6. But now the outputs are relatively consistent. The magnitudes of these outputs (figures 9.9b and 9.9c) also show another remarkable achievement that the output with two-branch system has increased twice in magnitude than those obtained with twin trap system (figure 9.8b and 9.8c). This shows that the two-branch traps are better than twin traps. However this circuit arrangement has the same disadvantages of shorter transient period and inconsistency in outputs as found in twin trap arrangement. Although this system does not require communication link etc, it suffers from maloperation of fault locators for low level signal threshold as described in sections 9.3i to 9.3vi. As far as reason for sudden change for higher output in two-branch trap system than that of similar case of twin trap requires further investigations.

Success of the research work is due to the peculiar super nature of present stack tuner from the fact that it uses virtual dynamic impedance of 400 ohms (surge impedance) at resonant frequencies instead

of constant value of R_0=400 ohms. At off-resonant-frequencies, the dynamic impedance of present stack tuner disappears completely by becoming closer to zero. It reappears only when it sees a resonant frequency for which it is designed.

Table 9.1a
Parameters of twin trap and corresponding stack tuner.

f_0 kHz	L_e mH	C_s pF	C_h μF	C_l μF	L_n mH	C_n μF	R_n m-ohms	L_s mH
10	.2	70	2.5310044	2.5350572	.02	12.665148	3.947842	3618.6137
15	.2	70	1.2504078	1.1265418	.02	5.6289546	8.882644	1608.2728
20	.2	70	.63287761	.63363752	.02	3.1662870	15.79137	904.65343
25	.2	70	.40505787	.40551179	.02	2.0264237	24.67401	578.97819
30	.2	70	.28129769	.28159790	.02	1.4072387	35.53058	402.06819
35	.2	70	.20667162	.20688431	.02	1.0338896	48.36106	295.39704

Table 9.1b
Parameters of two-branch trap and corresponding stack tuner.

f_0 kHz	L mH	C_s pF	C μF	L_n mH	C_n μF	R_n m-ohms	L_s mH
10	.05	70	5.066059182	.005	50.66059182	.24674011	3618.6137
15	.05	70	2.251581859	.005	22.51581859	.5551652476	1608.2728
20	.05	70	1.266514796	.005	12.66514796	.9869604401	904.65343
25	.05	70	.8105694691	.005	8.105694691	1.542125688	578.97819
30	.05	70	.5628954647	.005	5.628954647	2.22066099	402.06819
35	.05	70	.4135558516	.005	4.135558516	3.02266348	295.39704

where

$L_e = L_1 + L_2$ is effective inductance of twin trap
C_s, L_s = capacitance and inductance of series LCR stack tuner
L_n, C_n & R_n are parameters for parallel LCR stack tuner
L= inductance of two-branch trap
C_h, C_l = high and low resonant frequencies of the twin trap

9.3.ix Application as UNIVERSAL FAULT LOCATOR

A fault locator is universal, if and only if it detects all arcing and nonarcing type faults. Figure 9.10a shows complete single line arrangement of the 11 kV system including all fault locators representing universal fault type locators. Although the investigation and the explanation in this section are for the modal form, similar results in 1-phase method of this universal type of application of the fault locator can be obtained. Figure 9.10a shows that an extra capacitor of 1 uF is added at the centre of each fault locator between each phase and the earth. This capacitor forms a short-circuit for high frequency waves through which these frequencies easily drain to earth. When fault frequencies, after crossing closest trap of the closest fault locator to

a fault, meet first 1uF capacitor, all high frequencies pass (or drain) to earth, instead of travelling towards another side of the same fault locator. This makes high output voltage ratio of the two side voltages for the closest fault locators and absence of signals in rest of fault locators.

Two cases of line to earth faults are investigated, (i) solid line to earth fault and (ii) line to earth fault through ohmic resistance of 1000 Ω. Universality of the fault locator application is tested for fault localisation on both types of faults (the solid and the 1000 Ω) using one threshold level in modal form (this could also be extended to integration form of application which is not simulated here). Fault through 1000 ohms resistance represents low current level resistive faults. Although non arcing earth fault is investigated, this study equally applies to the arcing faults, as arcing faults and discharges create more noise frequencies than nonarcing resistive faults and these frequencies are continuous in time. The simulated results are shown in figures 9.10b and 9.10c. Modal output voltages for solid earth fault are shown in figure 9.10b. The output signal voltages in this figure show that the outputs from all stack tuners are negligible (nearly zero) except from the stack tuners close to and on both sides of the fault at YARB. The maximum fault signal in this case is approximately 15 volts. In this case a threshold voltage of 0.8 volts to 1.0 volt is enough. For a safety margin, threshold level of 1 volt is considered a level for the relay or the comparator described in section 9.3.i and 9.3.ii and shown in figures 9.1a and 9.2a. Fault localisation is done exactly in the same way as explained in sections 9.3.i and 9.3.ii. Figure 9.10c shows modal voltages for line to ground fault through 1000 ohms fault resistance. The maximum voltage in this case is approximately 4.5 volts. In this case the threshold level may be any value from millivolts to 3 volts. But threshold voltage level of 1 volt for relay operation is still comparatively appropriate. As 1 volt is the threshold level for relay operation in both the solid earth fault and the resistive earth fault and that the fault locator is capable of detecting all faults between 0 to 1000Ω resistance fault, this method of fault location is recommended and can be defined as universal.

9.4 Comparison of results

In this chapter various methods of the fault locator application are investigated. It is found that all application methods of the fault locator, are successful for low level fault detection, but these methods produce mal-operation by some relays at high level faults in all cases except two methods. The two methods which give successful fault location at low and high level faults are (i) the universal i.e. central capacitor tapping method and (ii) the raised to power signal processing method. By any one of these two methods, almost all arcing and nonarcing faults are detected. Raised to power method is totally signal processing based technique and needs microprocessor computing technique. The universal (or central capacitor tapped) method is an analogue method and it very efficiently determines the location of fault. This second method would also help in voltage regulation and power factor improvement in distribution network of countries like Pakistan where such capacitors are rarely used. In distribution networks where no capacitor banks are available a higher value of capacitance will produce much better results in fault location and benefit to the 11 kV distribution system.

The problem of transmission of information from fault locator to the primary station is solved by devising a new method. This method is called source-side multi-frequencies output type application. This method does not require any cable or wireless equipment to transmit fault signal to service station. This method shows that signal outputs are high and the method is reliable except that it suffers from variation of relative magnitude of signal output from different stack tuners. It is hoped that this method would provide the best results in future when this problem is understood and solved.

This chapter explains basic concepts of the fault locator application, modal mixing, comparison between protection system and fault location system etc. The author is sure that implementation of designing parameters along with suitable method of application described in this chapter, will enable a manufacturer of the commercially available fault locator to modify and use available products with very successful results.

Chapter 10

PERFORMANCE OF THE FAULT LOCATOR DURING ARCING EARTH FAULTS

10.1. Introduction

Electric arc has remained mystery and a source of great trouble in electrical distribution networks since its very early days, as reported by Davy in 1812 [45]. Until now there are numerous papers available on various aspects of the electric arc. Line to earth and line to line arcing faults are of major arcing concerns to Distribution Engineers. General characteristics, such as initialisation of arcing, arc extinction and v-i relationships governing the arc are similar in all types of arcings when considering the same media. Some common examples of arcings, in which these general rules are applicable, are arcings between (i) different parts of same machine windings, (ii) different live parts (or live part and earthed part) of same equipment, (iii) two sides of a live conductor while separating, such as in circuit breaker, fuse, loose joint and conductor breakage etc. If simultaneous arcing takes place at more than one place, behaviour of these arcs is mutually affected by one another. A famous case of this simultaneous arcing is circuit breaker opening during an arcing fault. In such case, the behaviour of the circuit breaker arcing together with the fault arcing has to be investigated simultaneously as will be reported in chapter 11.

Arcing phenomenon in a distribution system brings many disadvantages to power industry and its consumers. Arcs create noise frequencies in the distribution network, burn out electric conductors, damage equipments and machines, disturb electric services to consumers, reduce production, diminish earnings and ruin country economy. In order to avoid damages caused by arcing faults in distribution networks, early arc fault detection is necessary by an effective automatic fault locator, like this sample study in this report. In this chapter performance of the present fault locator under line to earth arcing fault is investigated.

Figure 9.10a of last chapter 9 is selected for line to earth arcing fault simulation study. The earth arcing fault takes place at YARB. The

resistance between YARB1 (or YARB) and earth is a nonlinear arc resistance. This nonlinear resistance is named R_p during high peak arcing current and RB during non-peak low arcing current on both sides of zero as discussed later in sections 10.3 and 10.4.

10.2. Initiation of arcing fault

Arcing is a process of electrical current flow through nonconducting medium (such as air or insulating oil) when molecules of the nonconducting medium break into ions and carry the electric charges (current) from one conductor (called electrode) to other conductor (or electrode). In arcing, energy is released in the nonconducting medium (usually air or transformer oil) and transients are produced in the distribution system. In the process of ionisation and conduction through molecules of the insulating medium, conducting material of the conductors also ionises and vaporises into the nonconducting medium by melting off of involved metal surfaces of the conductors. The arcing between two conductors (or electrodes) starts if and only if potential gradient between them is higher than the breakdown voltage of the air (or liquid) separating them. This condition is easily achieved (i) when separation between two 11 kV distribution conductors reduces to nearly zero by an accidental touching of the conductors followed by their small separation or (ii) when the air between them becomes ionised by one of several reasons given below;

i) frequent and repeated clashing of conductors in high winds.

ii) conduction between conductors (near earthed electric poles) due to humid climatic conditions of snow and rain.

iii) flash-over between conductors caused by such things as straw or twigs being blown across the lines, large birds spanning the lines as a result of their large wing spans, meat leftovers on conductors by birds, bird sittings with one foot on earthed pole and the other foot on live conductor, snake creeping, slippage of metal bar between two conductors touching simultaneously etc.

iv) accidental striking contact between live conductors for a short time caused by vehicle strike (such as a truck or an air craft) on live conductors, falling of a tree on conductors and uprooting of electric

pole carrying live conductors in rain and winds.

v) loose connections, causing overheating and minor arc formation, which over a long period of time worsens and ionises the air in the enclosed space enough to cause a spontaneous arc-over to ground or to another phase or neutral conductor.

vi) insulation failure between two conductors or conductor to earth through the failed insulation surfaces.

vii) conduction through cracks due to conductive dust typically from industry waste and contamination on insulators (such as wooden pole or insulation string).

viii) low current arcing between conductors and earthed metallic poles due to conducting salty particles in humid conditions near salty lakes, mineral mines, coastal areas etc.

ix) short circuit of 11 kV distribution conductors by falling of a conductor from other overhead line system.

x) over voltages resulting from lightning strokes over the conductors. In some cases the lightning occurs on the conductors and nearby metallic objects, in such a way that the over voltage create a very high arcing current flows through the conductors to earth via an arc over the insulators to the tower earthing.

10.3. Electric arc modelling

Ayrton [46] is probably the first who suggested, in 1902, air-arc voltage-ampere models for carbon and copper electrodes. The v-i characteristic arc model produced by him for copper electrodes in air, shown by equation 10.1, is still considered by some authors [47] along with its cyclogram.

$$v_{arc} = a + b/i_{arc} \quad \text{volts} \qquad (10.1)$$

where i_{arc} and v_{arc} are instantaneous current in amperes and voltage in volts

$a = \alpha + \Gamma . L$

$b = \beta + \delta . L$

L = length in cm

$\alpha = 30$ V

$\Gamma = 10$ V/cm

$\beta = 10 . a$ V

and $\delta = 30 . a$ V/cm

Following Ayrton, several other researchers investigated the arc conduction and published their findings in v-i arc models. Browne [48] (see figures 10.1 to 10.4) is probably the next most important researcher who investigated in detail v-i relationship. He produced cyclograms in volts/inch versus arc currents up to 20kA in 40kV circuit. The cyclogram in figure 10.3 shows that the arc voltage gradient, which Browne quoted from the work of Strom [49], is 25 V/inch. The 25 volts/inch, when converted into V/cm, becomes close to 10 V/cm which is used by several researchers, as will be discussed shortly. Warrington [50] experimentally determined the v-i arc characteristic given by equation 10.2.

$$V=8750L \;/\; I^{0.4} \quad \text{volts} \qquad \text{---------- (10.2)}$$

where V is rms arc voltage in volts and I is rms arc current in amperes, and L is arc length in feet. Rearranging the terms of equation 10.2, Warrington calculated the fault arc resistance by equation 10.3 given below.

$$R_{arc} = 8750L \;/\; I^{1.4} \quad \Omega \qquad \text{----------(10.3)}$$

This equation is effectively explained in the use of relay operations [51]. Equation 10.3 is roughly equal to $R_{arc}=292/I^{1.4}$ Ω/cm, which gives arc resistance of $R_{arc}=292\Omega$/cm in the region of 1 ampere, $R_{arc}=0.4628$ Ω/cm in the region of 100 amperes and $R_{arc}=0.0184$ Ω/cm in the region of 1000 amperes. Based upon his practical work and experience of other researchers in different parts of the world at that time, he also produced [51] arc resistance model in terms of arc current, arc length, wind speed and time, as shown in equation 10.4.

$$R_{arc} = [8750(L+3ut)] \;/\; I_{arc}^{1.4} \quad \Omega \qquad \text{---------- (10.4)}$$

where L is the arc length between conductors in feet, u is wind velocity in miles per hours and t is the duration after arc initiation in seconds [51].

Atabekov [52], from numerous investigations carried out by him in open air found that the arc voltage gradient for the arc length L between

two copper electrodes in air is independent of the magnitude of the arc current and that, on average, the arc drop amounts to 1.5 kV/m (or 15 V/cm) as given by equation 10.5.

$$V_{arc} = 1.5\ L \quad kV \quad \text{----------(10.5)}$$

where L is the length of the arc in meters, and V_{arc} is the arc voltage gradient in kV. He also found that the arc voltage gradient produced by high voltage networks heavily depends upon the magnitude of line voltage, wind velocity and time after initiation of the arcing. Atabekov's arcing fault resistance [52] is given by equation 10.6

$$R_{arc} = (1000\ L) / I_{arc} \quad \Omega \quad \text{----------(10.6)}$$

where I_{arc} is the arc current in amperes and L is the arc length in meters. This equation produces 10 Ω per cm per ampere.

Browne [48], Warrington [50,51], Atabekov [52], Latham [53], Cornick [54], and King [55) conclude that the voltage gradient per arc-length in air is variable from 10V/cm for heavy arc current to 800 V/cm for weak arc current and that the v-i characteristic depends on more than a dozen variables. These researches also show that under same conditions of network and arc length, if air is replaced by some other medium, the v-i arc model equation becomes different. These authors from their experimental, quantative and theoretical works proved the validity of their individual v-i model equations and cyclogram curves. Selection of cyclograms [48 to 59] are shown in figures 10.1 to 10.10. Figure 10.5 was prepared by Latham [53]. This figure presents a summary of several experiments of king [55] for long, free and vertical arcs in air. Latham [53] has made use of both King[55] and Engel[56] works. Latham compared his simulation work with King's practical work as shown in figure 10.5. This figure produces two types of arc behaviours. Currents below 70 amperes tend to have high and variable resistance whereas currents above 70 amperes have constant arc voltage gradient of 10 V/cm irrespective of current magnitude and variation of arc resistance. In fact Latham (fig.10.5) and Browne (fig.10.3) agree that V_{arc} is equal to 10 V/cm for both high and medium values of arcing current. Careful study of fig.10.5

shows that the arc resistance is (10V/cm/70amp=) 0.143 Ω/cm in the region of 70 ampers decreasing linearly to (10V/cm/1000 amp=) 0.01 Ω/cm in the region of 1000 amperes. Cornick's work [54] is detailed in figures 10.6, 10.7 and 10.8. He presents his findings by cyclogram in normalised arc voltage versus normalised arc current which he compares with the work of Strom [49] and others quoted in ref [54]. Figure 10.6 quoted from ref. [54] shows Strom's [49] arc voltage gradient of 10 V/cm for arc current ranging from 400 to 1400 amperes. Furthermore figure 10.7 also quoted from ref. [54] shows Dareniza's [60] arc voltage gradient of 450 V/cm for weak arc currents.

Based on experience of many previous researchers, Johns and Al-Rawi [57-58] and later Johns and Ritchi [59] carried out further investigations into generalisation of the arc model equations and produced a more comprehensive v-i arc model as given in equation 10.7. This equation covers both the light and heavy arc currents.

$$v_{arc} = 75\ i^{-0.4} \quad \text{V/cm} \quad \text{----------} \qquad (10.7)$$

In equation 10.7, v_{arc} is the instantaneous arc voltage gradient in V/cm for instantaneous normalised arc current (i) as a p.u. ratio. This equation is valid for current i between 0.15 p.u. and above in the increasing direction of the arc current to peak value and between maximum peak value to 0.38 p.u. in the decreasing direction of the arc current (see figures 10.9 and 10.10). Their cyclogram [57-58] shown in figure 10.9 shows arc voltage gradient of nearly 10 V/cm which is in good agreement with the work of Cornick [54], Browne [48], Latham [53] and King [55]. In equation 10.7, $i=i_a/I_p$ where I_p is the peak fault current computed from steady-state short circuit simulation [57-58] and i_a is the instantaneous actual arc transitory current, peak value of which is different in each cycle and in some fault inception it is much higher than I_p as mentioned earlier. Equation 10.7 represents region covered by the horizontal straight line shown as part of the cyclogram in figure 10.10 in the normalised units.

Figure 10.11 shows the peak part of the simulated steady-state short circuit current between terminals YARB and the earth where terminals YARB and earth are selected for arcing simulation (see figure 9.10a). A

low short circuit resistance of 1.0E-7 ohms was connected between the terminals YARB and the earth during this steady-state short circuit simulation. Value of I_p from figure 10.11 is 1643 amperes. Substituting for normalised value of i ($i=i_a/I_p$) into equation 10.7 and then replacing I_p by the known value of 1643.0 amperes, equation 10.8 is obtained.

$$v_{arc} = (75\ I_p^{0.4})\ i_a^{-0.4} \quad \{ = \quad (75^*\ 19.33\ )\ i_a^{-0.4}\}$$

$$= 1450\ i_a^{-0.4} \qquad \text{volts/cm} \quad \text{----------} \qquad (10.8)$$

In practice equations 10.7 and 10.8 are the same as they give the same result for the regions $0.15I_p$ (=246.45) to peak value of arc current i_a amperes and from peak value of arc current i_a to 0.38Ip (=624.34) amperes as per cyclograms of Johns et al [57-59] shown in figures 10.9 and 10.10. Equation 10.8 represents the arc voltage in terms of actual arc current i_a. Equation 10.7, contrary to equation 10.8, represents arc voltage in terms of normalised fault arc current i. Careful study of equation 10.8 for I_p=1643.0 amperes show that this equation does not represent the closely related cyclograms of Cornick, Latham, Johns, Browne as they all show arc voltage gradient of the 10 V/cm instead of 1450 V/cm shown by equation 10.8. This finding was confirmed by the EMTP trials. Use of equation 10.8 gave virtual zero crossing period prolonged for more than half of the total arcing period. Thus equation 10.8 failed to represent arc fault currents in its heavy and weak range of our study. There is a huge difference between equation 10.8 and the correct equation representing previous research works. In fact, in terms of Cornick's explanation [54], equation 10.8 may represent very low arc current in the range of microamperes, but surely it does not represent medium or high arcing currents. For this reason equation 10.8 is modified by equation 10.9, given below. Equation 10.9 uses 20 V/cm representing low and medium arc current instead of the 10V/cm used for medium and high values of arcing currents, as explained by almost all researchers and discussed above [48-61].

$$v_{arc} = 20\ i_a^{-0.4} \qquad \text{volts/cm} \quad \text{----------} \qquad (10.9)$$

where i_a is the actual arc current.

As equation 10.9 represents only medium values of arc currents in the v-i arc model, two more equations, one for arc current from 0 to $0.15I_p$ and another from $0.38I_p$ to 0 are required to complete the arc cyclogram. This is explained in the cyclogram of fig. 10.10. These equations are

$$V_{arc} = R_{rise} * 246.45 \quad \text{----------} \quad (10.10)$$

$$V_{arc} = R_{fall} * 624.34 \quad \text{----------} \quad (10.11)$$

Substituting V_{arc}=20 V/cm in equations 10.10 and 10.11 and rearranging terms of the resulting equations, the values of arc fault resistances are R_{rise}=0.081152363 ohms per cm and R_{fall}=0.032033314 ohms per cm arc length. In the present case, arcing is simulated between phase B at YARB and earthed mesh at a distance of 500 cm below the 11 kV power lines at YARB. The earthed mesh is for screening the communication lines as well as human safety in communication industry from accidental contact of falling 11kV power lines over the communication lines. In this case R_{rise} and R_{fall} for the 500 cm displacement of arcing path are 40.0 Ω and 16.0 Ω respectively. Using these arc path resistances, average value of RB is 28.0 Ω. This average value of RB is for arc current ranging from 0 to 435.40 amperes. The latter is average computed value of $0.15I_p$ and $0.38I_p$ for I_p=1643 amperes.

Dividing both sides of equation 10.9 by i_a and multiplying both sides by L, equation 10.12 is obtained.

$$v_{arc} L / i_a = (20 L i_a^{-0.4})/i_a \quad \Omega \quad \text{----------} \quad (10.12)$$

Substituting $v_{arc} L / i_a = R_p$ in equation 10.12, equation 10.13 is obtained

$$R_p = 20.0 L i_a^{-1.4} \quad \Omega \quad \text{----------} \quad (10.13)$$

The value of R_p in equation 10.13 is variable as a function of current and arc length and it varies from (20/435.4E+1.4=) 0.004041906 ohms/cm in the region of 435 amperes and (20/2000E+1.4=) 0.000478176 ohms/cm in the region of 2000 amperes, varying in between these two values non linearly.

10.4 Arc Simulation by EMTP

EMTP arc simulation between two points (in our case between YARB and earth) is carried out by EMTP's type-91 non-linear resistance and TACS statement of equation 10.13. Working of the EMTP program can be explained by the following steps:--

(i) increase time by δt. For first reading total time is zero.

(ii) close the switch between nonlinear resistance at YARB1 and the distribution network at YARB (see figure 9.9a).

(iii) calculate the value of arc resistance by TACS using EMTP's type 91-nonlinear resistance. To start, the initial arc current and arc resistance are zero. The value of arc resistance is calculated either from equation 10.13 as R_p or if the arc current is less than predetermined value of arc current (in this case 435.40 amperes) by a constant value of arc resistance RB. Note that direct calculation of Rp is incorrect or misleading as TACS uses one step old values of quantities. This will be explained fully in chapter 12.

(iv) construct network from branch cards

(v) calculate new value of source voltages of the constructed distribution network

(vi) calculate new values of i_{arc} and v_{arc} using TACS's (i.e. previous) value of arc resistance either RB or Rp such that arc current i_{arc} is adjusted according to new source voltages and the arc resistance (RB or Rp). The arc voltage is equal to multiplication of the arc resistance and arc current. Determination of I_{arc} and V_{arc} is implicitly carried out by EMTP.

(vii) repeat steps (i) to (vi) as many times as needed to complete arc simulation.

Using previously calculated value of RB=28.0 Ω derived for i_a=435.40 amperes and R_p from the above method, it was found that the value of the arc resistance R_p never reached a value lower than RB to the extent that arc current at peak value also remained very small and far from true shape of the arc current and the arc voltage. This defect was removed by the use of low value of RB equal to 2 Ω instead of previously calculated constant value of RB=28 Ω. With this value of RB=2 Ω, it is found that new peak value of R_p is approximately 2.0 Ω. It was observed

that use of RB equal to or less than 2.0 ohms did not influence the arc currents, arc voltages or the arc resistance R_p. Figure 10.12 shows cyclogram obtained from present values of arc current and voltage. Comparing the value of 2 Ω of the maximum arc resistance of present simulation with its value from equation 10.3 (Warrington's formula, between 0.0184 Ω/cm to 0.4628 Ω/cm), equation 10.6 (Atabekov's formula, 10 Ω/cm) and curve of figure 10.5 (Latham & King's formula, between 0.01 Ω/cm to 0.143 Ω/cm), it is found that this value of arc resistance for 500 cm arc length lies in between these values. The figure 10.13 shows the arc resistance R_p variation with time. This arc resistance is similar in magnitude and behaviour to the one obtained by Johns, Aggarwal and Song [61]. This confirms the validity of our arc simulation.

10.5 Performance of the fault locator

Figures 10.14 and 10.15 show arc simulated fault current and voltage respectively. These outputs are smooth and produce smaller arc transients than those shown in figures 10.16 and 10.17 taken from ref. [62]. The latter shows experimental results for arc performance. Comparison of simulated results with experimental results must show the level of accuracy of computation and the usefulness of the results. When comparing the two results, our results show less transients than those obtained from experimental results. Figure 10.16 [62] shows results of experimental arc voltage transients measured near the source and the load in a 40 kVA circuit. Close to the source, the source voltage is nearly sinusoidal, superimposed by arc transients. The voltage close to the load is entirely deformed. In both cases high transient waves are produced at the start in each half cycle of arcing. Figure 10.17 [62] shows test results of another case. In this case, the arc voltage shows that high voltage transients are produced from start to end of the arcing and after arcing. Similar situation is reported by other authors [12-13,21-25] where discharges (i.e. low level arcs) are detected continuously producing high frequency bursts.

50 Hz output results from simulation of arc, as shown in figures 10.14 and 10.15 though do not produce the expected high magnitude of transient frequencies, still their wave shapes adequately show the

expected arc current and voltage waveforms. Figure 10.18 shows fault locator outputs along with threshold level of 3 volts. Output from only two stack tuners MR2 of fault locator Loc2 and ML7 of fault locator Loc7 are higher than the threshold level of 3 volts. All remaining output levels are negligible (below 15 millivolts) and well below the threshold level of ± 3 volts. Thus the arc fault exists between two high outputs MR2 and ML7 which are the closest to the arc fault. High output signals from stack tuners closest to the fault confirm that the present fault locator is adequately capable of locating arcing faults.

Although fault discrimination is done by simple modal voltages, higher signal ratio can be achieved by raising the modal voltages or integration of raised modal voltage as explained in chapter 9.

10.6 Conclusion

Although arc transients produced by arc simulation in the present case of arc model by EMTP are less than expected compared to others, the output signals from stack tuners closest to the arc fault are reasonably high. Peak value of these voltages are about ± 15 volts. Signals from stack tuners away from fault are successfully low. Peak value of signal outputs from stack tuners away from fault is less than ± 15 milli-volts. Using threshold level of ± 3 volts, the present fault locator is capable of locating arcing faults.

Chapter 11

FAULT LOCATOR PERFORMANCE DURING (1) OPEN PHASE FAULT AND (2) THE CIRCUIT BREAKER OPENING AND RECLOSING

11.1. Introduction

Performance of present fault locator was investigated in chapters 7, 8, 9 and 10 for line to earth fault through zero and 1000 ohms resistance as well as arcing earth faults. In each case it was found that this fault locator locates the fault successfully. Simulation studies indicate that the maximum signal output at zero ohm fault resistance is ±15 volts and at 1000 ohms fault resistance is ±5 volts (see figs. 9.10b & c).

For proper operation of the present fault locator it must locate non-arcing open phase fault caused by breaking away conductor of the overhead 11kV distribution network. Separation of circuit breaker contacts with arcing phenomenon is similar to non-arcing open phase fault of a conductor as in both cases transients are produced and the fault locator detects each of these as a fault. Location of open phase fault is desirable whereas location of the circuit breaker opening and closing is not desirable. Operation of the fault locator on opening and closing of a circuit breaker is not in itself a defect but can create trouble. For this reason possible ways and means to stop operation of the fault locator on opening and closing of circuit breaker will be discussed in this chapter together with the performance of the fault locator towards the open conductor case.

11.2. Performance of the fault locator during open phase fault

Purpose of finding performance of the fault locator during an open phase fault is (i) to confirm successful operation of the fault locator during open phase fault and (ii) to establish relationship between operation of the fault locator during opening of circuit breaker and event of open phase fault. Simulation of circuit breaker by EMTP is done by

fixing switch timings and characteristics of nonlinear resistances, whereas simulation of an open phase fault is simply done by an opening of a closed switch connecting two sections of the same conductor.

Using circuit arrangement of figure 9.10a, an open line fault at YARB is simulated by opening a switch after 2.4 milli seconds from steady state operation. This switch is named YARB-TB3 in phase B at YARB. TB3 and T1FB2 form section 5 of the EMTP program (see chapter 2). Phase B voltage and current at the point of breakdown of the conductor are shown in figures 11.1a and 11.1b and in simple modal form the fault locator outputs are shown in figure 11.2. The threshold level is 3 volts. Only two outputs MR2 from Loc2 and ML7 from Loc7 exceeds the threshold level. These fault locators are the closest and on both sides of the open phase fault. Thus the fault locator locates the open line fault in the same way as it did locate the short circuit and arcing faults. It should be noted that the outputs from the two fault locators on each side of the open phase fault are higher than the corresponding value for line to earth arcing fault or line to earth (solid or resistive) fault.

11.3 Simulation of circuit breaker arcing

Figure 11.3 shows phase-B circuit arrangement of the 11kV system for the circuit breaker arc and line to earth arc simulation. It consists of a circuit breaker in close to source point JDBF. The circuit breaker model shown in this figure consists of two nonlinear resistances between JDBF and F1B1 and two switches PBB1-PBBB1 and QBB1-QBBB1. To simulate the circuit breaker functions, arc of the circuit breaker is simulated by the best possible opening and closing timings of the switches and use of nonlinear resistances according to equation 10.13. It is assumed that for general purpose, equations for the arcing earth fault and the arcing circuit breaker operation are the same, provided the air medium of conduction and electrodes are the same.

Procedure for simulation of circuit breaker arc is similar to that already explained for simulation of the arc fault in chapter 10 except careful use of (i) the circuit breaker switching times and (ii) the variable nature of distance between the contacts of the circuit breaker. Owing to the difficulty in plotting more than 16000 readings and

restriction to use small δt equal to 4.5 μ seconds, complete operation of the circuit breaker switching has to finish within maximum allowable time of 0.072 seconds. In practice 11kV system takes 5 to 10 seconds for a complete cycle, in average, from fault inception to the circuit breaker opening and its reclosing. Simulation of such long time by the EMTP is difficult. Present circuit breaker arc simulation, which is based upon the circuit breaker reclosing at 0.06 seconds and has total simulation time of 0.072 sec of the fault system, takes about 11 hours of 25 MHz PC computer. In order to check performance of the fault locator with time saving in computation, operation timings of a fast operating circuit breaker are selected. In order to show performance of the fault locator from opening of the circuit breaker to final reclosing, the opening and closing timings for this case are 0.02 sec and 0.06 seconds respectively. Complete details of switch timings for the circuit breaker arc operation are as below.

FTIME=0.0024 s, time for starting line to earth arc fault

COPEN=0.02 s, start of opening of the circuit breaker

CLEAR=0.04 s, time for complete opening of the circuit breaker contacts during arc

ECLEAR=0.0413 s, time for extinction of the circuit breaker arc

FOPEN=0.0415 s, time for line to earth fault clearing

CLOSE=0.06 s, time for reclosing of the circuit breaker

Time for which the circuit breaker is open following fault arc extinction is from 0.0415 sec to 0.06 sec. Note that arc extinction of the circuit breaker is achieved by opening both the PBB1-PBBB1 and QBB1-QBBB1 switches and line to earth fault clearance is achieved by opening switch YARB-YARB1. Final closing of the circuit breaker is achieved by closing switch QBB1-QBBB1, and using non-linear resistance QR1 equal to zero. As mentioned in switch timings, line to earth arcing fault continues from the circuit breaker arc extinction time 0.0413 seconds to fault arc extinction time 0.0415 seconds (a difference of 0.0002 sec). This is due to induction of voltages from phase A and phase C into phase B (secondary currents). Arc faults during this period (of 0.0002 sec or 100th part of a 50 Hz cycle) does not exactly follow secondary arc pattern explained by Johns and Al-Rawi [57-59] for high tension lines. Reasons for this simplified simulations are 1) secondary arcing is negligible in 11kV system, 2) this

research is not meant for study of the secondary arcs, 3) even if secondary arcs were simulated, they would have made no or little difference in fault locator performance as the noise frequencies during 11 kV secondary arcs is less than those obtained from opening or closing of circuit breakers, 4) as time duration for secondary arcs is very small, their effect can not be visible in any output due to the smaller magnitude of the secondary arcs in 11kV systems than the primary arcs already included and 5) arcing is prolonged for this period of 0.0002 sec by the arcing subroutines of the EMTP to match the arc extinction at zero current crossing.

In simulation of the circuit breaker arcing, maximum separation between two contacts in the present case is assumed 5cm. Circuit breaker separation starts at time COPEN with 0 cm separation between the contacts and then increases linearly with time till it is fully open with 5 cm apart at the time CLEAR=0.04 seconds.

11.4. Performance of the fault locator during opening and reclosing of the circuit breaker operation

Currents and voltages at different nodes are obtained for a period before, during and after line to earth arcing fault and circuit breaker operation. Figures 11.4a to 11.4c show source phase currents. The source current in phase B (see figure 11.4b) during nonarcing and full opening period, of the circuit breaker, is zero. Figures 11.4a, 11.4b and 11.4c show small magnitude of high frequency transients. Figure 11.4d shows the arcing fault current between node YARB and earth. The corresponding fault arc voltage between YARB and earth is shown in figure 11.5e. Figure 11.4d show that the magnitude of transients in the current wave form is small. Figure 11.5a to 11.5c show source terminal voltages. These voltages show clear variation in magnitude due to effect of start of phase B to earth arcing fault and circuit breaker's arc extinction and reclosing which are clearly visible by high frequency transients superimposed on the 50 Hz waveforms. Figure 11.5d to figure 11.5f show node voltages at YARA, YARB and YARC respectively. The voltage at YARB is the line to earth arc fault voltage. It shows that it contains relatively less transients during arcing period than the transients introduced to it

during opening and closing of the circuit breaker. Voltages across electrical terminals of the circuit breaker of the same phase 'B', are shown in figures 11.5g and 11.5h. Figure 11.5h is expanded version of figure 11.5g. These figures show that arcing voltage across the circuit breaker contacts is only up to ± 200 volts, but the recovery voltage increases rapidly during nonarcing open circuit breaker period. Non-arcing open circuit voltage across the circuit breaker contacts is very much oscillatory. Figure 11.5i shows phase B voltage between feeder side of the circuit breaker F1B1 and earth. It shows presence of high transient frequencies at arcing timings and nonarcing open circuit period of the circuit breaker. The corresponding variation of arcing resistances are shown in figure 11.6a at fault and b at circuit breaker. The simple modal form output voltages from all stack tuners are shown in figure 11.7. The figures show that due to the series arcing of the circuit breaker, the output signals from stack tuners closest to the circuit breaker have increased several times which when compared with the fault signals from the other types of arcs and faults are much higher. These results show that the stack tuners of the fault locators closest to the circuit breaker are capable of locating the opening and closing of the circuit breaker as if these events were faults. Depending upon the value of the threshold level, these fault locators on both sides of the circuit breaker and arcing fault location give higher outputs and locate fault and operation of the circuit breaker as if it is a fault. The output shows that the signal increases after each time the circuit breaker opens or closes. Fault locators are supposed not to operate under circuit breaker opening and closing.

11.5 Ways and means to stop circuit breaker influence on the fault locator.

Three methods were investigated for stopping of the circuit breaker influence on the fault locator during its opening and closing operation. Two methods out of the three failed to succeed. The successful method is called shunt capacitor by-passing. This method along with the two failed methods are discussed in the following paragraphs.

The shunt capacitor bypassing method uses the technique of

connecting a shunt capacitance of 1 uF between each terminal of the circuit breaker and the earth, in a similar way to the technique already being used in universal fault location methods. This method is chosen in application for the present fault locator arrangement as in figure 11.3, whereby a 1uF capacitor is connected at the centre of each fault locator. This arrangement by-passes high frequency transient components to earth by short circuiting circuit breaker terminal nodes JDBF and F1B1 to earth at high frequencies. At power frequency this capacitance would add to voltage regulation and power factor improvement as discussed previously. The modal output voltages obtained from various stack tuners are almost the same as shown in figure 10.18. This shows that the output voltages from stack tuners closest and on both sides of the operating circuit breaker (with circuit breaker terminals connected through 1 uF) are zero as if the circuit breaker was either absent or had not operated. This proves that this method is absolutely effective in stopping circuit breaker operation, influencing performance of the fault locator at the time of its opening and closing. Comparison of results from figure 11.7 with the results of figure 10.18 confirms the success of the solution.

The two other methods which failed were (i) series capacitor bypassing and (ii) blocking traps. Series capacitor bypassing was carried out by connecting a capacitance of 1 uF between the terminals of the circuit breaker. The blocking traps were carried out by connecting traps of both sides close to circuit breaker terminals. Both of these methods failed to stop propagation of transient high frequencies from circuit breaker to the fault locators. These two methods failed due to absence of short circuit path between the circuit breaker terminals and earth. This concept was confirmed by installing traps away from the circuit breaker terminals through a section of a distribution line. The mutual capacitance of this line section, between the conductors and earth, helped the trap circuits to achieve the blocking of high frequencies. Again this method is not satisfactory and is not suggested here.

11.6 Conclusion

In this chapter, studies for the performance of the fault locator under open phase fault and circuit breaker operation are presented. In

both cases, the fault locator without the bypassing capacitors locates opening of the phases as a fault. Our proposed, remedy to this tendency of producing high frequency output signals in closeby fault locator, is the connection of the aforementioned shunt bypassing capacitors.

In this case of shunt bypassing capacitors, terminals of the circuit breaker at high frequency become short circuited to earth. This modification in the circuit breaker application has enabled the present fault locator to become a perfect fault locator with no side effects. Although the results produced in this chapter are only in modal form, other forms of results can be derived and used successfully, depending upon the need and accuracy required by the desired individual method.

Considering the system economics, the addition of the 1.0 μF shunt bypassing capacitor could be of a station poster or additional insulator to a pole mounted transformer. This is left for future investigations.

Chapter 12

SAFETY & PERFORMANCE OF THE FAULT LOCATOR DURING LIGHTNING STROKES

12.1 Introduction

Striking of lightning strokes on overhead distribution conductors directly, or indirectly from reflections of the ground, produces enormous discharges of electric energy from the charged clouds to the electric conductors and the electric conductors to earth, resulting in a surge of huge current and then from the conductors to the ground. Due to the earthing tower foot resistance, flow of the electric current causes generation of an enormous over voltages between the live conductors and the ground. In absence of a low resistance path, this surge voltage could jump up to hundreds of thousands of volts. This high surge voltage directly hits all distribution equipments and destroys almost all the equipments. As the proposed fault locator has to be installed in series and parallel with the overhead distribution conductors, it is quite possible that this equipment will be damaged by such lightning impulses unless it is properly protected by an enforced method (lightning arrestors).

The main purpose of this chapter is to investigate protection of the fault locator during lightning. The protection is usually achieved by a lightning arrestor. During this investigation lightning surge voltage across the fault locator with and without surge arrestor is studied. If the surge voltage across any terminal of the fault locator is found to be greater than a predetermined standard accepted value, the fault locator is said to have been damaged by the lightning strokes on the conductors. If the voltage during lightning or thereafter is kept at or below the standard accepted rated surge voltage by use of the surge arrestor, the fault locator is said to have been protected. Simulation is carried out in such a way that the lightning strokes do not destroy fabrication of the fault locator (i.e. its parameters do not change), and therefore its performance during lightning with and without surge arrestor operation remains unaffected. This directs us to find the magnitude of the output

signal in both cases and hence the output signals will be used to investigate the behaviour of the fault locator.

12.2 An over view to damages caused by lightning

A lightning stroke produces impulse of current of steep front and slowly decaying tail. On the basis of numerous investigations, it has been found that the average peak value of lightning current is 20k amperes at 1.2 μ seconds from start of the stroke. This value is now accepted as an International Standard for shape and size of the lightning stroke. This current when passes through impedance path from the conductor to the earth, it generates a very high voltage drop across the tower and earthing impedances. Consequently, the normal a.c. line voltage is raised to a very high magnitude immediately at the point hit by the stroke and ground. This high surge voltage travels in all the possible directions. As the value of the lightning current and overvoltage is very high, though it lasts for short time, it usually results in real havoc and serious damage to almost all equipments connected on the distribution conductors by the travelling wave of the violent lightning impulse voltage. Expensive repair, costly shutdown and time consuming replacement of equipments become essential part to restore the service.

12.3 Use of surge arrestors for over voltage protection

To reduce damage by lightning, lightning arrestors are installed close to terminals of equipment to be saved. The substation equipments which are usually protected include transformers, circuit breakers, relays, condensers, reactors, and in some cases electric meters and switches. In the future the fault locator may play an important role in fault location and protection. It also has to be protected from lightning and other switching surge voltages. This protection can be provided by the installation of surge arrestor between each terminal of the fault locator and earth. Solid earth path to a lightning arrestor provides the necessary low resistance path which it uses to shunt the huge excessive current to keep a constant rated voltage across the terminals. In normal conditions the surge arrestor draws no current. However when a lightning stroke

strikes on a distribution conductor and as soon as the surge voltage across the surge arrestor increases beyond the predetermined level of voltage (called rated voltage of the surge arrestor), the surge arrestor starts conducting by keeping a constant voltage drop across it. Lightning arrestors are designed to clip off the high impulse surge voltage peaks so that the clipped-off voltage peak does not exceed 1.8 X (peak standard voltage value) which in present 11kV system equals to $1.8*6.35*\sqrt{2} = 16$ kV per phase. Furthermore in practice all equipments including the fault locator connected to the distribution system and its substations should be designed to withstand impulse voltages of 2.3 X (peak rated line to line voltage) which in the present case for the 11kV system equals to $2.3*11*\sqrt{2} = 36$ kV. Consequently the arrestor diverts a substantial part of the surge energy to ground. The truncated impulse wave which travels beyond the arrestor then has a peak per phase value of only 16kV. This impulse can easily be borne by the fault locator which if properly designed withstands a higher impulse voltage of 36kV than this truncated peak voltage of 16kV. As lightning may take place at anyplace, surge arrestors are required to be installed on both sides of each fault locator. The surge arrestor clips off the impulse voltage by decreasing its resistance. Whenever the line voltage, due to lightning increases beyond the rated voltage of the surge arrestor, then the surge arrestor adjusts its resistance automatically to allow flow of excessive current to maintain its rated voltage. This process of keeping maximum voltage equal to a constant rated voltage across the surge arrestor saves the fault locator and other equipments on the line.

12.4 Lightning impulse

Recorders of transient disturbances [63] on distribution systems have shown that a lightning stroke is a pulse of steep wave-front and relatively slow decaying tail as shown in figure 12.1. This figure shows the agreed International Standard shape and magnitude for the voltage produced by the Lightning Current Impulse. This wave attains its peak value of 20k amperes at 1.2 μ seconds after initiation of the lightning arc and falls to one half of the peak value in 50 μ seconds. A simple lightning current impulse of the fig.12.1 is expressed by equation 12.1.

$$i = I_{max} (e^{-\alpha t} - e^{-\beta t}) \text{ ----------} \quad (12.1)$$

where $\beta > \alpha$, and α, β, I_{max} are constants.

Following International Standards, a lightning impulse has a peak current of 20 k amperes at the peak 1.2 μs. Therefore differentiating of equation 12.1 at 1.2 μs and equating to 0 at peak value, the resulting equation is shown by equation 12.2.

$$di/dt = 0.0 = I_{max} (-\alpha e^{-\alpha t} + \beta e^{-\beta t}) \text{ ---} \quad (12.2)$$

By running a FORTRAN program for equations 12.1 and 12.2, a set of appropriate values of α, β, I_{max} of the equations 12.1 for the lightning stroke impulse current are 14340.0, 4000000 and 20486.87 respectively.

12.5 Derivation of model equation for surge arrestor

If V_{ref} is the desired reference voltage for clipping off of the lightning impulse voltage and V_{ars} is the actual arrestor voltage achieved, then theoretically for ideal performance of the lightning arrestor, the two voltages should be equal, as given by equation 12.3.

$$V_{ars} = V_{ref} \text{ ----------} \quad (12.3)$$

Dividing both sides of equation 12.3 by I_{ars} and substituting for V_{ars}/I_{ars} by R_{ars}, the resulting equation 12.4 is given below.

$$R_{ars} = V_{ref} \; I_{ars}^{-1} \text{ ----------} \quad (12.4)$$

Since the 11kV system has 8981.46V per phase peak voltage, the cutoff reference voltage V_{ref} is given by equation 12.5.

$$V_{ref} = 1.8 * (8981.46 \text{ V}) = 16000 \text{ V} \text{ ----------} \quad (12.5)$$

Substituting V_{ref} = 16000 V of equation 12.5 into equation 12.4, equation 12.6 is obtained.

$R_{ars} = 16000 / I_{ars}\ \Omega$ ---------- (12.6)

Equations 12.4 and 12.6 are the surge arrestor model equations and voltage V_{ref} is the safe maximum voltage for the fault locator.

12.6 Representation of the surge arrestor in the EMTP

Equation 12.4 or 12.6 is similar to arc equation 10.13 which is discussed in chapter 10. A practical surge arrestor follows equation 12.6 by cutting off high impulse voltage across the surge arrestor at a constant voltage V_{ref}. Voltages below V_{ref} are not changed by the surge arrestor.

The surge arrestor simulation given by the present EMTP is found defective and produces wrong results. This error is due to (i) use of TACS to calculate variables, in our case nonlinear resistance R_{ars}, from previous step voltages and currents and (ii) inability of TACS to exchange TACS's equations within iterations. TACS uses EMTP's output which are calculated one step behind. This means if the running cycle of EMTP is using time t seconds, then the currents and voltages being used in TACS at time t are of the time $(t-\delta t)$ i.e. one step back. This is confirmed when running our programs and in itself from the Rule Book of the EMTP. In other words unless some caution is taken, those using TACS can expect any error level depending upon the type of simulation and step size δt.

Simulation of surge arrestor clipping off voltage starts by previously known value of arrestor current I_{ars} (as all TACS values are old by 1 step of execution) and its substitution in equation 12.6. If the arrestor current I_{ars} is less than a predetermined value, in this case 1.0E-10 amperes, then TACS device No.60 acting as IF statement of FORTRAN, makes I_{ars} equal to 1.0E-10.

Suppose lightning stroke voltage of 37kV appears for the first time at surge arrestor node at time t and that at time $(t-\delta t)$, voltage at the surge arrestor node in previous execution of the EMTP program was less than V_{ref} with I_{ars}=0. Similar to the arc simulation, explained in section 10.4, computation of R_{ars}, I_{ars} and V_{ars} by the EMTP proceeds as below.

(i) increase time from $(t-\delta t)$ to t.

(ii) close switches of the branches containing nonlinear resistances for

the surge arrestors. In present case, they are already closed.

(iii) use TACS to calculate non-linear resistances. The TACS will check the value of current I_{ars} by device No. 60, which in the present case will change the value of 0 to 1.0E-10. This conversion of values is necessary to avoid overflow of the R_{ars} value in equation 12.6. Then TACS computes the value of R_{ars} from equation 10.6. For I_{ars}=1.0E-10, equation 12.6 gives R_{ars} (16000/1.0E-10)= 1.6E+14 Ω.

(iv) construct network from branch cards. This approach is complex and unknown to us, but for simplicity we use Thevenin Theorem at the surge arrestor nodes. By excluding the surge arrestor resistance R_{ars} of 1.6E+14 Ω, we assume the Thevenin's impedance of 300000 Ω. This high value of impedance is merely to explain of how the EMTP works. The value of this impedance may be equal to surge impedance of the lines (300-600 ohms).

(v) calculate new value of the network voltage at time t. In the present case the voltage at the surge arrestor nodes is already assumed to be 37kV.

(vi) calculate new value of I_{ars} and V_{ars} from the value of R_{ars} and circuit parameters. In our case, the total impedance (R_{ars}+R_{Th}) of the circuit using Thevenin theorem at the surge arrestor node is (1.6E+14 + 3E+5) =1.600000003E+14 ohms. The instantaneous value of I_{ars} is

I_{ars} = 37000 / 1.600000003E+14 = 2.312499996E-10 amperes

and the value of V_{ars} is

V_{ars} = I_{ars} * R_{ars} = 2.312499996E-10 * 1.6E+14 = 36999.99993 volts

This value of V_{ars} is not the 16kV, expected from the above EMTP procedure.

Now consider computer FORTRAN program, if it were in step (vi) of the EMTP procedure shown above, it will calculate the values of R_{ars}, I_{ars} and V_{ars} as given below.

```
VREF = 16000
VTH  = 37000
RTH  = 3.0 E + 5
DO 1 I=1, 10000
```

```
      RARS = VREF / IARS
      RTOTAL = RTH + RARS
      IARS = VTH / RTOTAL
      A = ABS(RCHECK - RARS)
      IF ( A .LT. 1.0E-3 ) GOTO 2
      RCHECK = RARS
1     CONTINUE
2     CONTINUE
```

By this simple program, correct values of R_{ars}, I_{ars} and V_{ars} will be calculated for the surge arrestor model equation 12.6, where by the assumed surge voltage of 37kV is now truncated at exactly 16kV.

EMTP does not directly use FORTRAN's DO loop within the iterative method to calculate correct value of I_{ars} and R_{ars}. For a sudden high increase of impulse surge voltage, EMTP calculates I_{ars} on the basis of previous value of R_{ars}. Thus instead of showing proper chopping of lightning surge voltage across the surge arrestor, a higher surge arrestor voltage $V_{ars} >> V_{ref}$ is computed. This computation in FORTRAN programming is corrected by repeated iteration in execution of equation 12.6 and other relevant equations till each of R_{ars}, I_{ars} and V_{ars} stabilizes and become almost equal in each execution. This is not possible in current EMTP version. EMTP considers the single computed value of R_{ars} from equation 12.6 accurate and final. Use of EMTP's single calculated value of R_{ars} can not be corrected by other means. This approach of EMTP in arc modelling creates oscillations and unnecessary deviation from true value of V_{ref}. This makes computed value of V_{ars} greater than V_{ref} during ascending of impulse voltage.

The second error in the EMTP simulation is in the use of a switch in series with the nonlinear arc resistance R_{ars} in the surge arrestor model, as shown in the figure 12.2. This is required by the TACS in contrary to common FORTRAN programs, for which it does not need switch JDB2-SB to calculate I_{ars}. In EMTP, the value of I_{ars} can only be computed if a switch is available in series with the nonlinear branch. Figure 12.2 allows the use of EMTP to calculate I_{ars} by TACS output/input statement No.91 (for more information see EMTP Rule Book). The instantaneous value of the arc current I_{ars} is needed for calulation of R_{ars} from equation 12.6. But the use of switch in EMTP, springsup its own problem. This problem is that EMTP finds some difficulty in the formation of the Y matrix of the network to include the nonlinear resistances of the surge

arrestor, as declared by the EMTP in itself during diagnosis. For this reason the EMTP internally adds a high resistance in the range of 1.0E+6 to 1.0E+10 ohms (the exact value depends on other parameters of the network). This is in parallel with the nonlinear resistance of the surge arrester between terminal SB and earth. The EMTP informs us about this added resistance during diagnosing. This added resistance though of high value, do draw some current across the surge arrestor branch. This increases the value of the surge arrestor current at node SB (i.e. I_{ars}=SB) to use in equation 12.6. This uncertain situation of the internal resistance is corrected by deliberate addition of known value of resistance (in this case equal to 1.0E+7) between SBV and earth, as shown in figure 12.3. Now this resistance value is known and the current drawn by this resistance is correctly calculated by FORTRAN like statement (SBV / 1.0E+7) in TACS. This current (SBV/1.0E+7) is subtracted from total current SB at node SB (see figure 12.3). The correct value of surge arrestor current I_{ars} is given by equation 12.7.

$$I_{ars} = SB - \frac{SBV}{1.0E+7} \qquad (12.7)$$

where SB is the total current at terminals SB computed by the EMTP while SBV is the total voltage at SBV terminal. It must be noted that computation of I_{ars} in equation 12.7 is done in TACS which is of the one step old value of SB and SBV.

The surge arrestor model shown in figure 12.3 is the most possible accurate model for the EMTP simulation to investigate surge arrestor and fault locator performance. However, due to the wrong type of software (the EMTP), simulation of the surge arrestor produces incomplete clipping off of the peaks and the surge arrestor model is defective.

12.7 Circuit arrangement for simulation of lightning

Figure 12.4 shows phase B circuit arrangement of the 11 kV distribution system for simulation of lightning. Three separate surge arrestors, one on each phase, are connected at each phase terminal of the 3-phase fault locator all along the distribution conductors. Figure 12.4 shows connection of the surge arrestor for the safety of the fault locator

Terminals where individual surge arrestors are installed for simulation purpose, are JDA2, JDB2 and JDC2. Lightning arc takes place on YARB and spreads over to YARA and YARC and the pole to ground. The metallic pole has an assumed low value of 2 ohms foot resistance between node STRIKE and earth. The low value of resistance between STRIKE and earth is assumed to keep low value of surge voltage. The lightning strike source of current is generated by impulse source Type 15 of the EMTP with the aforementioned I_{Max}=20486.87, α=14340.0 and β=4000000. The lightning current impulse obtained by these constants is shown in figure 12.5a with figure 12.5b showing its expanded version. This EMTP version of source has two terminals (see Rule Book for details), the earth and LIGHT. This current source starts generation of the lightning current impulse from TIMEX=1.9E-6 seconds (TIMEX is reserved name for EMTP's running time in a program). Simulation of lightning strike on the conductors and the pole takes place at TIMEX=3.0E-6 seconds by short circuiting terminals YARA, YARB, YARC, STRIKE with LIGHT. This lightning short circuit occurs from TIMEX=3.0E-6 to TIMEX=0.14E-3. The lightning voltage created at and after strike across terminals YARA, YARB, YARC, STRIKE and LIGHT is shown in figure 12.5c. Opening of these nodes takes place without permanent damage to the conductors or the pole by no alteration of the parameters presenting them in the simulation.

12.8 Performance results of the surge arrestor

The node voltages during lightning, with and without the arrestor are shown in figures 12.6 to 12.9. Figure 12.6a shows the lightning voltages at nodes YARA, YARB & YARC. Expanded along time axis, these voltages are shown in figure 12.6b. These voltages show that the lightning arc produced is in the range of 40 kV. The high voltages at these nodes travel in both direction along the distribution lines and reach nodes JDA2, JDB2, and JDC2 on the source side and T1FA2, T1FB2 & T1FC2 on load side (see figure 12.4). The high voltages at these nodes are shown in figures 12.7a, 12.7b, 12.8a and 12.8b. The maximum magnitude of these voltages is once again approximately 40kV. Nodes JDA2, JDB2, JDC2, T1FA2, T1FB2 & T1FC2 are terminals of the fault locator. The rated maximum safe voltage for the fault locator is 16 kV. Voltages higher than 16kV at these

nodes, destroys the fault locator. Thus the present voltages in the range of 40kV (without surge arrestor) surely have had destroyed the fault locators.

In order to save the fault locator from high lightning surge voltages, lightning arrestors are now assumed installed at JDA2, JDB2, & JDC2. No surge arrestor is installed at T1FA2, T1FB2 and T1FC2 for simplicity in programming and discussions. Surge arrestors are connected between fault locator terminals and earth.

Simulation of surge arrestor was carried out with different values of δt. These δt values are 4.5E-6, 5.625E-8 and 1.25E-8. Nodal voltages across surge arrestors at JDA2, JDB2 and JDC2 are shown in figure 12.9a, 12.9b and 12.9c respectively. Each figure shows 4 outputs for the same node but with different δt. The first curve (i) shows the surge voltage without the arrestor. The second curve (ii) shows surge voltage with surge arrestor simulated by δt=4.5E-6 seconds. The third curve (iii) shows the surge voltage simulated by δt=5.625E-8 seconds. The final fourth curve (iv) shows surge voltage across the surge arrestor simulated with δt=1.25E-8 seconds. Comparison of curve (ii) with other curves shows that the surge arrestor model has not succeeded in operation with δt=4.5E-6. The magnitude of the voltage across the surge arrestor with δt=4.5E-6 is almost equal to the voltage without the surge arrestor shown in curve (i). Curve (iii) and curve (iv) obtained by low values of δt show that the surge voltage across the surge arrester has been clipped-off but not smoothly. Again comparison of curve (iv) with curve (iii), shows that ripple peak in curve (iv) with smaller δt is smoother and less than that obtained with higher δt.

The stated no operation of the surge arrestor (curve (ii)) described in the above paragraph is due to the inability of the EMTP to simulate an accurate surge arrestor model as described in section 12.6. If iterative techniques were used properly within EMTP, correct truncation of the surge arrestor voltage would have been obtained. As lightning impulses are steep and in average attain their peak value in 1.2 micro seconds, a δt less than one tenth of 1.2 microseconds produces the truncation of the surge voltage. Instead curve (iv) of figure 12.9a is obtained with δt=1.25E-8 seconds which forms 96th part of 1.2μsec. Execution of the EMTP with this small value of δt takes a very long time

to complete 16000 readings. For example, total length of the curve (iv) in figure 12.9, with δt=1.25E-8, is obtained by running the EMTP program for about 11 hours (PC 25 MHz). Furthermore reduction in δt showed very little change. After running several runs of the EMTP with several low values of δt, it is concluded that "the EMTP with the smallest possible δt equal to 0.9E-99 seconds will still not be able to get a smooth curve."

However for general purpose curves (iii) and (iv) can be considered truncated at required reference voltage of 16kV. Since 16kV is the rated safe voltage for the fault locator. Use of the surge arrestors would certainly save the fault locators.

12.9 Performance results of the fault locator

As explained in sections 12.6 and 12.8, because the terminal voltages across the surge arrestors are not smoothly chopped off and consequently the fault locator output during same duration of time and operation are wrong, the output voltages from the fault locators with the surge arrestor can not be relied upon. Just to see how the surge arrestor reduces impulse voltages across its terminals, δt equal to or less than 5E-8 seconds is required. But with this small δt, the voltages across the surge arrestors still contain very sharp spikes of voltages.

Performance of the fault locator was investigated after removing 1 μF capacitance from centre of each twin trap mentioned in chapter 11 in figure 11.3. The system after removal of the capacitors is shown in figure 12.4. Two sets of readings of the fault locator outputs are obtained, (i) with the capacitor banks and (ii) without the capacitor banks. With the capacitor banks connected at nodes FA2, FB2 and FC2, the signal output voltages MR71,MR72, MR3, ML3, MR4, ML4, MR5, ML5, MR6 and ML6, as shown in figure 12.10a, become almost zero due to shunting of high frequency signals through the capacitor banks to earth. These output sigal voltages from the fault locators are obtained without surge arrestor at the fault locators, but with the capacitor banks connected. These show that the fault locator has successfully located the fault between Loc2 and Loc7, as only two outputs from stack tuners belonging to Loc2 and Loc7 close to the fault are much higher than rest of the outputs from stack tuners away from the fault. The two output voltages in modal form in figure 12.10a are

in the range of ±95 volts. The outputs shown in figure 12.10b are obtained when no capacitor bank is connected in the 11kV network. It shows the output signal voltages in modal form. These voltages are also obtained without surge arrestors across the terminals of the fault locators. The output voltages show that only two outputs from Loc2 and Loc7 are very high in the range of ± 95 volts. Other output signal voltages lie within ± 16 volts. Difference between output signal voltages of figures 12.10a (with capacitor banks) and 12.10b (without capacitor banks) is that output signal voltages in the former case, from the fault locators away from the capacitor banks, on opposite side of the fault, reduces to nearly zero where as in the latter case, they are not. If the threshold voltage level is 30 volts, only two fault locators Loc2 and Loc7 operate and show location of the fault. The 10kHz signal output voltages in figure 12.10b, without capacitor banks, during lightning fault shows that if the threshold level is lower than 5 volts, almost all fault locators will locate the fault between them. This is wrong operation of the fault locator and must be corrected. This maloperation of all fault locators in the case of lightning strokes with small threshold voltage level is avoided by insertion of 1μF capacitor in the middle of the twin traps, as proved from the results in figure 12.10a, in which case presence of the capacitor banks makes signal voltages MR71, MR72, MR3, ML3, MR4, MR5,ML5, MR6 and ML6 nearly equal to zero or as explained in chapter 9 by using 1 μF capacitors in the middle of the twin trap does the same thing.

Fault locator output signal voltages with the surge arrestor operation are not shown here for (i) having wrong results at δt=4.5E-6 and (ii) having very low voltage output signals, that is only for few cycles of 10 kHz at δt=5.625E-8 and below. Fault locator output signals obtained with deltat=4.5E-6 are equal to the fault locator outputs without the surge arrestor shown in figure 12.10b, and are therefore wrong. Similarity of the fault locator output signal voltages at δt=4.5E-6 sec, with and without surge arrester, is due to unsuccessful chopping-off of the impulse voltages with δt=4.5E-6. The small deltat equal to 5.625E-8 and 1.25E-8 gave reasonable truncated voltages across the surge arrester but the fault locator signal output voltages with the small values of δt were only for few milli-seconds, that is not fully developed. When these output signal voltages were examined, they could not locate the fault. In order to avoid

misleading interpretation, these output signal voltages are not shown here.

12.10 Conclusions

1. The results show that the surge arrestor is capable of clipping off the lightning impulse and is therefore capable of protecting the fault locator from the lightning. Use of surge arrestor between the fault locator terminals and earth definitely protects it and is strongly recommended.
2. The fault locator during lightning is capable of locating the fault. The modal output signal voltages during lightning but without arrestors are about ten times greater than the output voltages obtained in other types of faults. With low threshold level of signal voltage, maloperation by the high output signal voltages during lightning can be avoided by connecting a capacitor of about 1 μF value at the centre of each fault locator.
3. Surge arrestor modelling by EMTP requires special attention. For instance, to get reasonable results, very small δt of at least 5E-8 is required. The output with this small δt still contains very sharp spikes. In future the EMTP should better enable surge arrestor simulation.
4. To provide comprehensive studies for the effect of surge arrestors upon the performance of our fault locator, a dedicated faster EMTP would be required to cater for such small sampling times.

Chapter 13

SENSITIVITY ANALYSIS FOR THE EFFECT OF A MARGINAL CHANGE IN THE PARAMETERS OF THE FAULT LOCATOR

13.1 Introduction

Due to the delicate construction of the fault locator parts and high selectivity requirement for blocking of the resonant frequency together with the narrow band of frequencies around it by the trap circuit and filtration of these by the stack tuner, the fault locator needs (i) accurate designing of its parameters, (ii) simulation of its performance (iii) precise manufacturing and (iv) field testing before offering it to practical commercial use. All these are necessary to ensure reliable performance of the fault locator. Almost every component of the fault locator is important and needs careful attention in each stage to make it withstand the rough and tough nature of the outdoor installation described in chapters 3, 4 and 5. Components of the parallel resonant circuit of the stack tuner take small current and develop small voltages upto 100 volts during average lightning strokes. Those stack tuners can be manufactured as small units in lumped components. Similarly the series inductor of the stack tuner is a lumped parameter and could be small in size as the current is low. These small sizes of the lumped parameters can be manufactured precisely as well. The only components which bear a lot of current and voltage of 11 kV are the power coils L_1 & L_2, power capacitors C_1 & C_2 and the series stack tuner capacitor C or C_{stack} shown in figures 3.1 and 3.2. Location of capacitance of the series stack tuner capacitor and its distributed nature makes it more vulnerable than any other component of the fault locator. The capacitance of the series stack tuner capacitor is formed from a metallic coating and central metallic tube separated by an insulating plastic tube. The metallic tube holds the 11kV distribution conductor. The distribution conductor and the tube form one side of the capacitor while the other side is the metallic coating. A terminal is brought from the metallic coating to connect it with the

series inductor L or L_{stack} and the parallel resonant circuit of the stack tuner (see figure 3.2 and figure 10 of the attached CIRED paper). It is likely that the capacitance of the series stack tuner capacitor may change due to one or other reason. These reasons include (i) change in dimension caused by temperature variation, (ii) change in dimension due to change in size of diameter of the distribution conductor inside the metallic tube, (iii) deformation of the metallic coating due to aging, bending or breaking and (iv) manufacturing defect etc. To ensure satisfactory performance of the design and manufacturing of the fault locator, it must be thoroughly measured for its components at the centre frequency f_0. For any change in measured value of any one or more components, performance of the fault locator must be examined before putting into service.

In this chapter effect of the magnitude of the series stack tuner capacitor C_{stack} (figure 3.1, 3.2 and 5.1) on the performance of the fault locator is reported. This study assumes that the only component which changes from its design value is this capacitor.

13.2 Circuit arrangement

In order to compare output from two sides of a fault locator in a realistic way, central capacitance of the twin trap fault locator is removed. This is necessary to find the difference in outputs from both the sides of the same fault locator. In the presence of the central capacitance (see figure 9.10a), the second side of the fault locator will not receive noise frequencies. The required outputs from both sides can be achieved either by removal of central capacitance from the twin-trap or use of two-branch trap described in chapter 9. In this chapter a simple two-branch trap instead of a twin trap is preferred in the fault locator as the former is as efficient as the latter but uses low value of inductance of the power (or trap) coil as described in section 9.3 viii. The circuit arrangement of figure 13.1 shows application of this arrangement. This arrangement is similar to figure 9.9a. The trap circuit of this fault locator uses 0.05 mH inductance of the power coil instead of a total of 0.2 mH inductance of the power coil as suggested in the twin trap circuit (see table 9.1 in section 9.3 viii). This reduction in inductance magnitude to its one fourth value is essential to reduce

capital and running costs of the fault locator. Table 13.1 shows design details of the fault locator components shown in figure 13.1.

Table 13.1

DESIGN OF TRAP CIRCUIT (Two-branch type)					
R_{trap} ohms		L_{trap} mH		C_{trap} uF	f_0
0.00005 ohms		0.05 mH		5.066059182 μF	10kHz
DESIGN OF STACK TUNER (Series/parallel type)					
C_{stack}	L_{stack} mH	L_n mH	C_n μF	R_n ohms	f_0
70E-6	3618.613	0.005	50.66059	2.467401E-4	10kHz

Other reasons for selection of two-branch trap instead of twin trap include (i) simplicity of the two-branch trap in its component design, circuit arrangement and presentation in the EMTP program and (ii) requirement for further investigations on the fault locator using two-branch trap. Further investigations on the two-branch trap fault locator are assumed necessary to complete " the basic purpose of this research which is to find the best possible fault locator (or locators) for the 11kV distribution system". This purpose would be accomplished, if and only if, all possible versions of this fault locator are examined. For this reason partial investigations on the two-branch trap type fault locator carried in chapter 9 needs confirmation.

13.3 Procedure for simulation and study

Using the designed parameters shown in table 13.1, it is first found that if these parameters of the fault locator are capable to locate a fault. If confirmation of such successful results is obtained, further simulation for different values of C_{stack} are carried out to examine the effect of variation on performance of the fault locator.

With the design parameters shown in table 13.1, performance of the fault locator simulation at 10 kHz is shown in figure 13.2. It shows the outputs of the fault locator from various stack tuners. These outputs show that this design (first used in chapter 9) of the fault locator works very well and the fault locator is capable of locating the fault at YARB

between Loc2, Loc3 and Loc5. This performance of the fault locator has been obtained with the series capacitance value of C_{stack}=70pF of the stack tuner and for solid earth fault at YARB.

The fault locator is now tested for four different values of series stack tuner capacitance. The values are 70pF, 70.2 pF, 70.5 pF and 71 pF. This provided simulation of 4 different output voltages from each fault locator. The fault locator performance in all these cases is achieved under same conditions of the circuit arrangement and fault simulation. Each time the fault is created by short circuiting switch at YARB with ground. The output is collected from across the parallel branch of the stack tuner.

Figure 13.3 compares modal output voltages from three stack tuners of Loc2, Loc3 and Loc5 closest to the fault. The fault was created between fault locators Loc2, Loc3 and Loc5. The results show that there is a very wide variation in output voltages for small changes in the capacitance. At capacitance value of 71 pF the fault locator output voltages show that each stack tuner output is low and almost same in magnitude from all places. This fault locator loses its property of discrimination for fault location at C_{stack}=71 pF. This figure also shows that the fault locator is capable of locating fault within the variation of ± 0.5 pF. But this variation forms only ± 0.7% variation. This shows that for successful operation of the fault locator, attention must be given to the required accuracy of parameters even with weather conditions.

13.4 Conclusion

Performance of the fault locator with a change from 70 pF capacitance value to 70.2 pF shows that it is still capable of fault location. The fault locating property is reduced when the capacitance value of 70.5 pF or beyond is reached. Nevertheless it is still capable of discrimination upto 70.5 pF.

Difference in output voltages from four different simulations using small change each time in the series stack tuner capacitance shows that this fault locator requires attention for any variation in parameter values. It is capable of operating successfully if the series stack tuner capacitance changes are within ± 0.7%. However for the capacitance changes

greater than 0.7%, performance of the fault locator becomes unreliable. It shows that for successful performance, the fault locator needs (i) high quality design of the circuit components (ii) high quality manufacturing and (iii) necessary safe guard from damage in the outdoor installation so that its installation in the outdoor performance does not change any component value for all rough use.

The successful performance of the fault locator with simple two-branch trap circuit proves that (i) the present fault locator as well as its stack tuner are efficient, (ii) the fault locator can work on low values of inductance of the power coil (equal or less than 0.05 mH), (iii) two-branch trap is simpler and may prove better efficiency than the twin trap.

Chapter 14

PERFORMANCE OF THE FAULT LOCATOR AT DIFFERENT RESONANT FREQUENCIES

14.1 Introduction

For different reasons the fault locator may be required to operate on different resonant frequencies other than 10 kHz. In such cases, the fault locator components are replaced by new values. These new values are determined exactly by the same procedure as described for 10 kHz. After designing the fault locator, a power system analysis is required to ensure performance of the fault locator with the new component values. Thus before manufacturing of the fault locator in full, determination of its performance is essential.

In this chapter performance of the fault locator for different resonant frequencies f_0 is determined. The fault locator will be examined for 10kHz, 50 kHz and 90 kHz using two-branch trap circuit for simplicity.

14.2 Procedure for simulation

Figure 13.1 shows the circuit arrangement for the investigation into performance of the fault locator in this chapter. This circuit arrangement uses two-branch trap. The design parameters of the fault locator for different resonant frequencies are shown in table 14.1.

Table 14.1a

R_{trap} ohm	L_{trap} mH	C_{trap} μF	f_0
0.00005	0.05	5.066059182 μF	10 kHz
0.00005	0.05	2.026423673E-1 μF	50 kHz
0.00005	0.05	6.254394052E-2 μF	90 kHz

Table 14.1b

C_{stack} μF	L_{stack} mH	L_n mH	C_n μF	R_n ohm	f_0 kHz
70E-6	3618.613	0.005	50.6605900	2.467401E-4	10 kHz
70E-6	144.7445	0.005	2.02642400	6.168503E-3	50 kHz
70E-6	44.67424	0.005	0.06254394	1.998595E-2	90 kHz

For each resonant frequency, branch cards representing these components of the fault locator are replaced by appropriate designed values from table 14.1 and that is for each of the six fault locators. Then branch cards representing overhead distribution conductors are separately computed from JMarti Subroutine and then the output cards of this subroutine are used to replace the same in the main program. The program is then checked and rechecked for node names, values of branch cards, source voltages, δt, TMAX etc. When the program becomes properly checked, it is run with δt=4.5E-6 and TMAX=0.072 seconds.

14.3 Performance of the fault locator at different f_0

Figures 14.1 to 14.3 show the fault locator performance at different resonant frequencies respectively. The signal output voltages of the fault locator with resonant frequencies of 10 kHz are shown in figures 14.1. The 10kHz signal output voltages from stack tuners closest to the fault are at least 8 times greater in magnitudes than the signal output voltages from stack tuners away from fault. The 10 kHz signals are spread over 80 ms and beyond.

Figure 14.2 shows signal output voltages from the fault locators at 50 kHz resonant frequency. The 50kHz signal output voltages show that the output voltages from stack tuners closest to the fault are amplified and with different ratio (closest to farest signals). In case of Loc2, the output from stack tuner close to fault is 5 times greater than the output from stack tuner away from fault. In case of Loc3 and Loc5, the output from stack tuner close to fault is only 2 times greater than the corresponding output from stack tuner away from the fault. Comparing these signals with those of 10kHz of figure 14.1, signal MR2 of Loc2 is twice larger of MR2 signal at 10kHz whereas ML3 and ML5 from Loc3 and Loc5 at 50 kHz are only 1.2 times larger for the same corresponding signal ML3 and ML5 from Loc3 and Loc5 of 10kHz. This shows that the signal output voltages from stack tuners closest to the fault at 50kHz are greater than the corresponding voltages at 10 kHz but with uneven increase. From figure 14.3 signal output voltages obtained for 90 kHz resonant frequency show similarity with the results from 50kHz. Unequal increase in growth of the output signals for high resonant frequency are a cause of concern,

although each time signal output voltages from stack tuners close to fault are greater than corresponding values from stack tuners away from fault. Figure 14.3 also shows that the output voltage magnitudes are shorter in time than those from 10kHz. The 90 kHz signal output are from about 1.5 ms to about 7 ms instead of about 1 ms to beyond 80 milli seconds in the 10 kHz case. This shows that higher the resonant frequency, shorter is the duration of sustaining their output voltages. Figures 14.1 to 14.3 show that the fault locator with each resonant frequency behave different but each time the fault is located precisely.

These output results with different f_0 show that for better signal discrimination and higher output voltages, higher resonant frequencies are not necessarily better. At very high frequency f_0, inconsistency in output signal voltages from the closest stack tuner worsens and is a cause of great concern. Due to the smaller gain in signal output voltages from some of the stack tuners, high resonant frequency is not necessarily advantageous. Increase in frequency from 10kHz to 90 kHz has also resulted in decrease in time duration for sustaining output signal from 80 ms in 10kHz to just 7 ms in 90 kHz.

14.4 Conclusion

Figures 14.1 to 14.3 show that higher output signal voltages are obtained at higher resonant frequency and vice versa, but the increase in signal is inconsistent. For this increase, the signal strength at higher resonant frequency is not constant for all outputs. This may cause maloperation of relays, recording equipment, indicating equipments and alarms. Another disadvantage of high f_0 is that the higher resonant frequency reduces period of signal availability (i.e. period of sustain). Reduction of time of the signal availability decreases efficiency of the fault locator. The third disadvantage in use of higher resonant frequency f_0 is interference with broadcast frequencies or even aviation. For these reasons proper selection of the resonant frequency is very important. The study of this chapter shows that resonant frequency of 10 kHz gives better flat gain results than those obtained at higher resonant frequencies. Since the principle of the fault locator is capable of locating fault at any resonant frequency, it confirms that this fault locator is versatile

in its application. Its use as universal fault locator, i.e. with a capacitor at centre of the fault locator, makes it suitable and reliable sensor for fault location in all situations of faults.

Chapter 15

CONCLUDING REMARKS AND FUTURE WORKS

15.1 Concluding remarks

In this thesis, design, working principle, testing, and methods of application of a successful fault locator are fully described starting with basic concepts. Performance of the fault locator is examined at each stage of design by computer simulation for different types of problems. Faults include solid line to earth fault, line to earth fault through 1000 ohms resistance, line to earth arcing fault, open conductor fault and lightning stroke effects. In all the situation studies carried out, performance of the fault locator shows that it successfully locates the fault with high accuracy. Measurements of the fault locator are based on co-ordination of two types of analogue filters working on common resonant frequency. The first filter (called trap circuit) blocks a band of frequencies while the second filter (called stack tuner) detects existence of the same band of frequencies. Depending upon the method of its application, if any of the stack tuners detects the signal (i.e. it gives an output signal to operate an alarm etc), a fault is located. Performance of the fault locator is also investigated for different resonant frequencies. Results at higher resonant frequencies show that higher gain is achieved at these frequencies. These results confirm that the fault locator is reliable at all these frequencies and for all earth fault types.

Performance of this fault locator under variation of its capacitance is tested to be reliable within ± 0.7% variation. This confirms that the fault locator is capable of operating in mild rough climatic conditions. But if the variation of this component is greater than 0.7%, this fault locator would be less capable of fault location. Sensitivity of remaining components are believed of less vulnerable than this capacitance. Each component requires careful design and manufacturing For rough use, where the components values change, then a twin trap version with 1 μF capacitor may improve its performance.

Purpose of this research is to modify and improve an existing commercially available fault locator. This fault locator model in its commercial form is found unable to locate a fault. This research proves that the commercially available fault locator suffers from its poor design of series LCR resonator circuit which is unable to filter the desired frequencies for wideband noise frequencies. For this reason signal output voltage from each stack tuner in the old design needed re-filtration to separate wanted signals from unwanted signals [1-9]. For this purpose external filters with a minimum of 9 stage Butterworth digital form in addition to two aliasing filters were used. With all these efforts [1-9] the output from closest stack tuner to the fault was only ± 250 milli volts. And this voltage output was obtained for solid earth fault and line to line fault of a distribution system at no load on its terminals (i.e. the condition of high transients).

Present research [10-11] as described in this thesis for the first time includes not only terminal loads, but also line tappings, power factor improvement and voltage regulating by capacitor banks, arcing line to earth faults, circuit breaker arcing, open circuit fault and performance during lightning strokes. In all cases the present fault locator locates each fault and it does this very successfully with high accuracy. The output signal voltage from line to earth fault through 1000 ohms resistance show that the signal output from the closest stack tuners is greater than ± 5 volts. This result is very much encouraging as this fault locator is capable of locating high resistance faults. For this reason, performance of the fault locator can be tested practically without causing disturbance in the circuit. This confirms that low level arcing faults can also be located without further signal processing.

Study of air circuit breaker is included in this research to study its effect on performance of the fault locator. The study shows that closing and opening of the circuit breaker is detected by the fault locator like a fault. This mal-operation of the fault locator on opening and closing of the circuit breaker is alleviated by the use of shunt capacitors connected across terminals of the circuit breaker and the earth.

Study of the protection from lightning strokes is included in this research to confirm proper safety of the fault locator. The study shows

that the fault locator is well protected by connecting surge arrester across each terminal of the fault locator.

This research includes all major useful applications of the fault locator including signal processing. Connection of 1 uF capacitance at the centre of the fault locator converts this fault locator into a universal fault locator. No fault locator at present or in future would beat the universal fault locator as it operates on the analogue principle. However it can be converted into digital version easily, if still required. For those who prefer signal processing method, a new method of application is described. This method is called 'raise to power 10 and integrate'. With this application of the fault locator, it never fails in locating a fault. The problem of transmission of information from fault locator to the remote location (primary or control station) is solved by the method called source-side multi-frequencies type application of the fault locator described in chapter 9. This method does not require any cable or wireless equipment or extra dc or ac voltage source to transmit the fault signal.

As described in this thesis, initially the research work on this fault locator was carried by El-Hami for his PhD under the supervision of Johns. Although El-Hami and Johns [1-3] produced successful results for fault location, the output signals were of low magnitude. Initially this failure for low output voltage was assumed from narrow band of the trap circuit. This is also reflected by the use of twin trap circuit in this thesis. But in chapter 7, it became apparent that the failure to obtain high output signal value from the fault locator was due to failure of old fashioned series LCR stack tuner and not from the trap circuit. In chapter 9 and onward it was fully realised that the fault locator does not necessarily require a wideband twin trap. For this reason, a narrow band two-branch trap was introduced in chapter 9 and onward to show performance of the freshly designed fault locator. The output results in these chapters proved that the cause of failure in the research by others was due to the stack tuner and not due to the trap circuit. This is confirmed by the use of the narrow band two-branch fault locator which provides successful results. The achievements in this design includes (i) use of low value of inductance 0.05 mH power coil instead of 0.2mH inductance power coil which was proposed in the twin trap circuit and (ii) the high outputs. Surprisingly 0.05mH inductance coil filter gives higher output

than those obtained with 0.2mH trap circuit. Furthermore design of the two-branch trap circuit is much simpler than the twin-trap circuit. With this new design principle, the author then advances few steps further with his simple design in the studying sensitivity of the fault locator in chapter 13 and effect of different resonant frequencies f_0 on performance of the fault locator in chapter 14. Results of these two chapters confirm that the fault locator is working perfectly in this simple design and has high output for almost all frequencies. The results show that performance of the fault locator is very much sensitive on variation of resonant frequency and higher output is obtained at high frequencies to a certain level and then becomes irregular in output. The results show higher output signal voltages are obtained at higher resonant frequency and vice versa, but the increase is inconsistent. An other disadvantage of high f_0 is that the higher resonant frequency reduces period of signal availability. Reduction of time of the signal availability decreases efficiency of the fault locator. The third disadvantage in use of higher resonant frequency is interference with broadcast frequencies or even aviation. This study shows that resonant frequency of 10 kHz gives better flat gain results than those obtained at higher resonant frequencies at 50kHz and 90 kHz.

This thesis contains details of all design works, with their necessary explanation and argument on almost every aspect of the fault locator. It forms a comprehensive handbook for this fault locator. Theory, design and application of this thesis can be used to modify circuit arrangements of the commercially available fault locator. The fault locator can conveniently be tested for high fault resistance of 1000 ohms or more. As the simulation computer test results show that this fault locator is capable of locating high resistance faults, testing of this fault locator on practical 11kV distribution line with 1000 ohms fault will not produce any problem to normal operation of the 11kV system and that the fault locator can conveniently be tested.

15.2 Future works

The useful and successful work described in this thesis can be put into useful application in 3 areas ;-

(i) fault location

(ii) protection

(iii) application to other type of faults

(iii) communication

15.2.1 Fault location

The research work described in this thesis clearly speaks for the fault location. The available commercial fault locator may be modified accordingly, and tested on site for commercialisation. As this fault locator is capable of locating high resistance faults and low sparking arcs, tests on physical fault locator will not disturb performance of any existing 11kV system.

15.2.2 Protection

The output signal from this fault locator is high reliable and fast in response. It can best be used to protect sensitive equipments and lines by direct connection to relays. Proper calibration will make a relay to operate above certain level of fault.

15.2.3 Application to other type of faults

The developed fault locator is tested by simulation tests for line to ground fault through zero and 1000 ohms fault resistance, arcing earth fault and open phase fault. Other faults which cause severe damage to the distribution system are (i) 2 phase to ground (2ph-Gr) and (ii) phase to phase (ph-ph) faults. These faults are left to others for future investigations.

15.2.4 Communication

Design of the stack tuner filter is based upon entirely new concept. This concept has never been used before. By this design, impedance as well as bandwidth of the filter can be fixed. Both properties are very important in load-matching and band selection. This filter has also provided virtually zero output outside its selected band. Impedance-frequency response of this filter for the narrow bandwidth is close to

ideal square pulse. Comparing this work, with the work of previous authors (1-9) for similar faults, the other fault locators have different stack tuner filter. Our present filter has higher output and clear filtration, though in previous works multisection Butterworth filter has been used. This filter requires only few components in contrary to Butterworth and all other filters, yet it is the most effective in filtration than those described any where in a book or a research journal. This filter could be useful in all branches of communication, electronics, control and protection such as TV, radio, telephone, computer, camcorder, navigation, power systems and other types of sensor applications where detection by a selected narrow bandwidth over selected impedance and selected resonant frequency of the filter is required.

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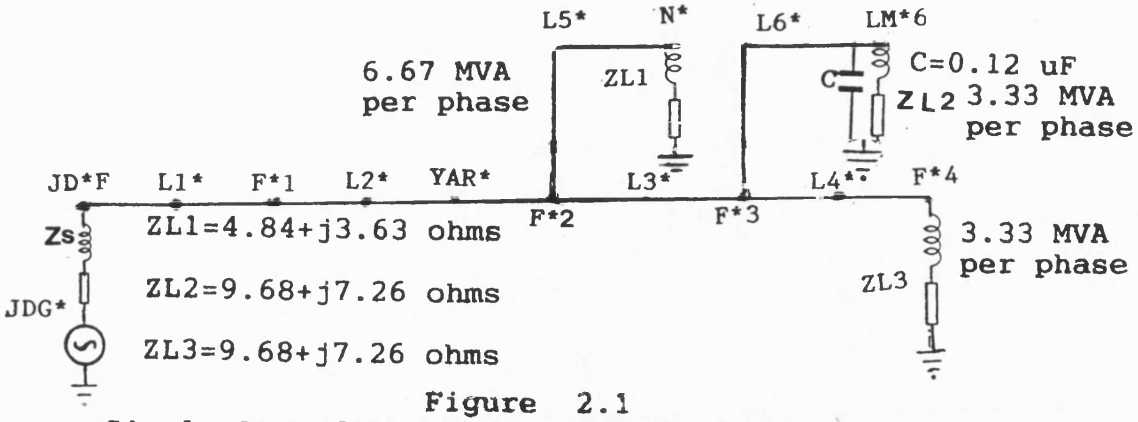


Figure 2.1
Single line diagram of selected distribution network for installation of capacitor banks and fault locators

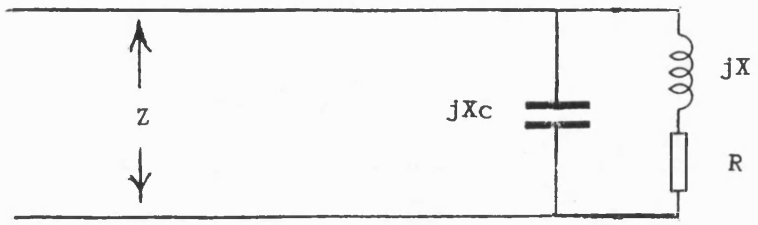


Figure 2.2
A generalised case of p.f. improvement

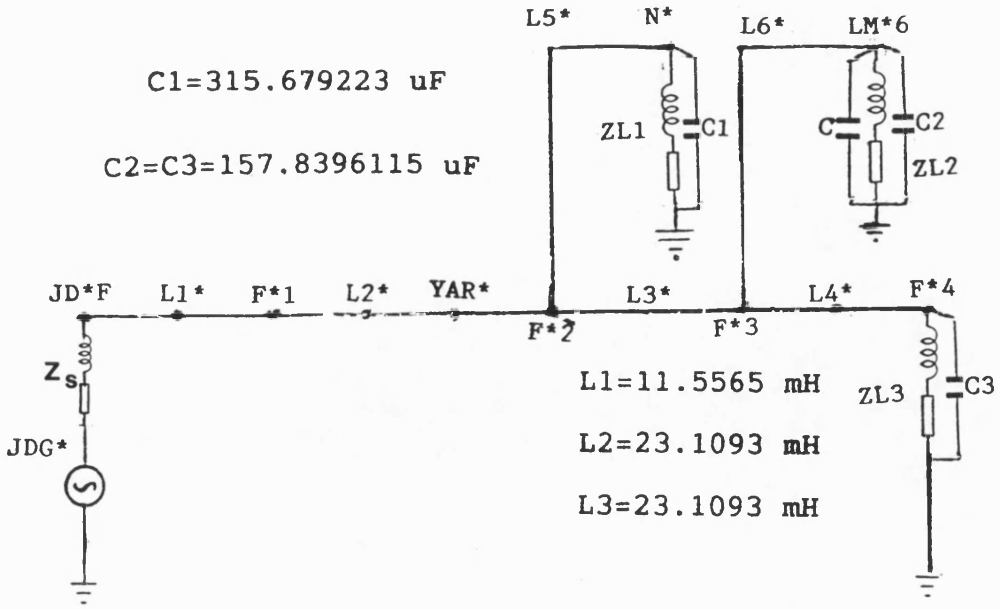


Figure 2.3
A distribution network with capacitor banks close to inductive loads

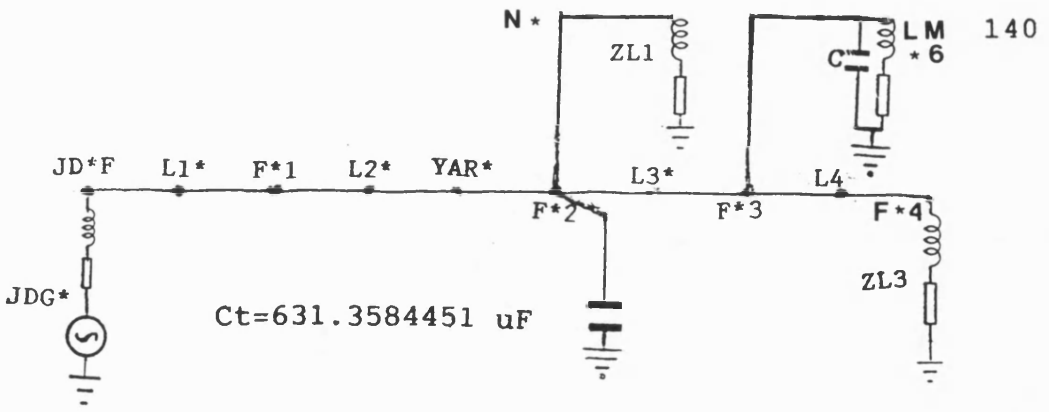


Figure 2.4
A distribution network with capacitor bank at load center

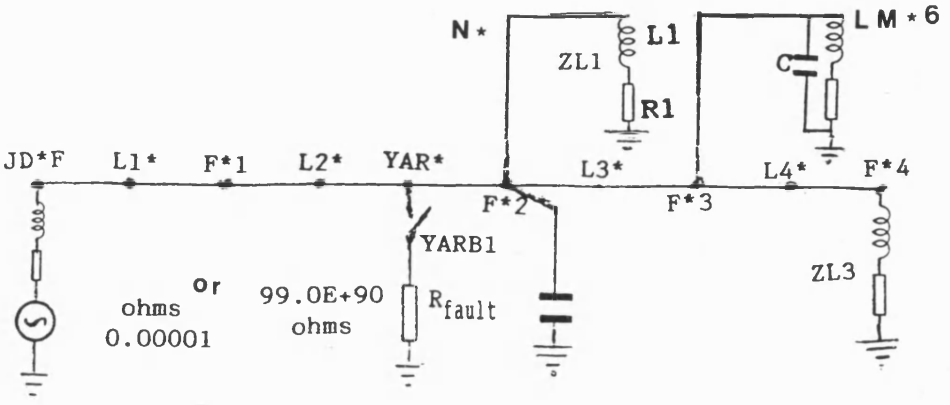


Figure 2.5
Single line diagram of selected distribution network for steady-state analysis (R_{fault} = 99.0E+90 ohms) and transient behaviour (R_{fault} =0.00001 ohms)

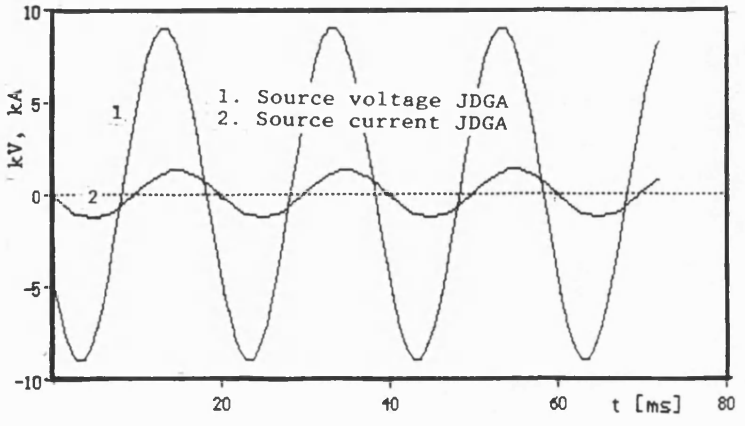


Figure 2.6
Steady-state source voltage and total distribution network current

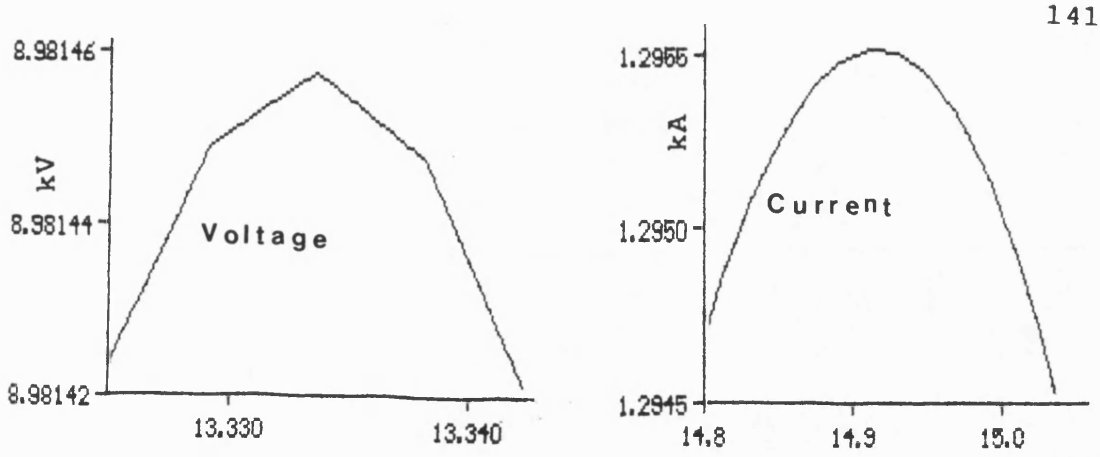


Figure 2.7
Expanded steady-state source voltage & current JDGA at peak

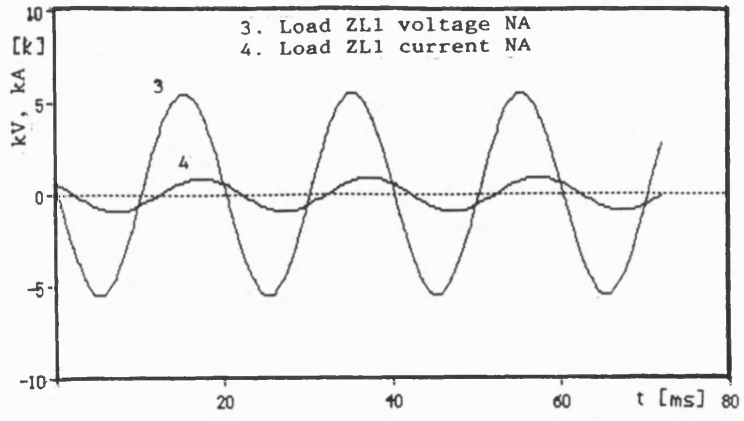


Figure 2.8
Steady-state voltage and current at load node NA

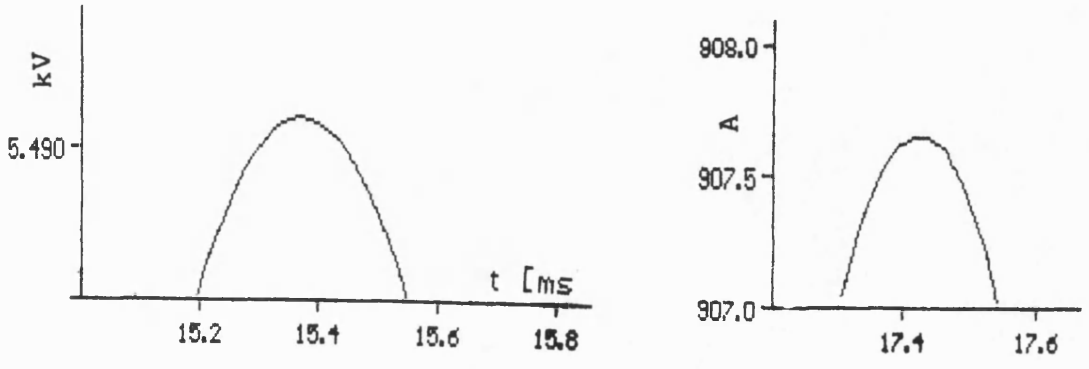


Figure 2.9
Expanded steady-state load voltage & Current NA at peak

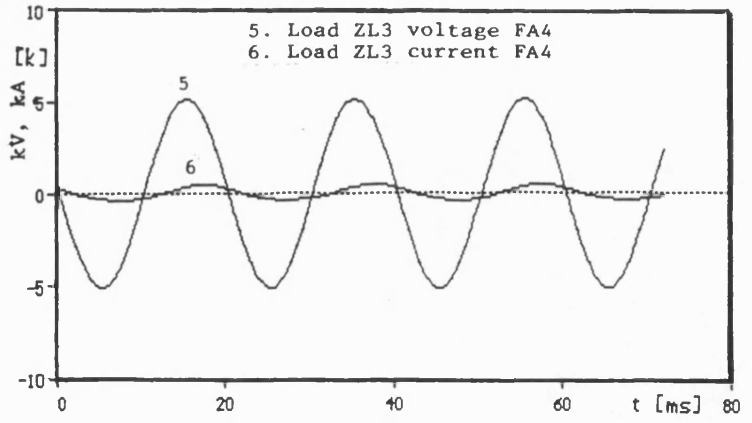


Figure 2.10
Steady-state voltage and current at load node FA4

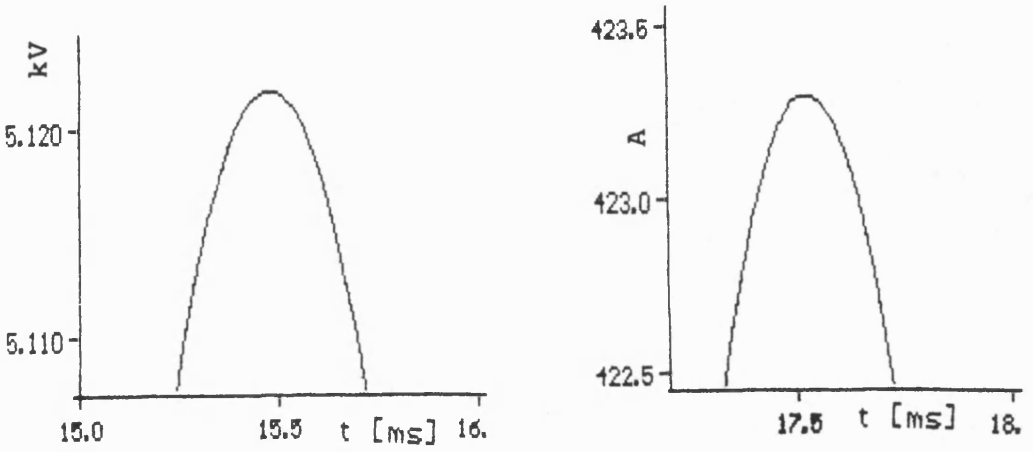


Figure 2.11
Expanded steady-state load voltage & Current FA4 at peak

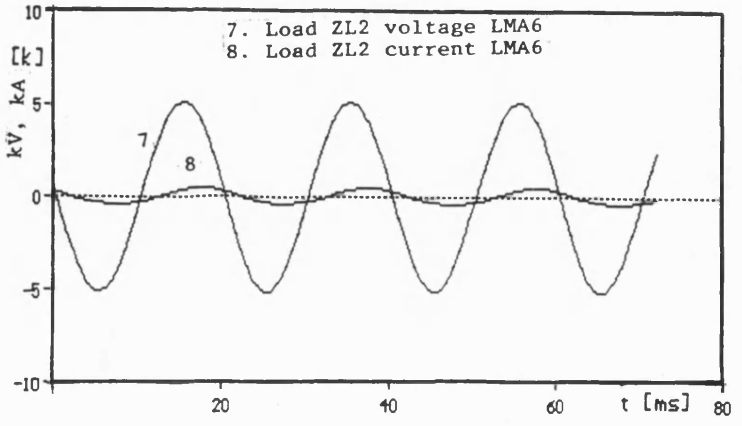


Figure 2.12
Steady-state voltage & current at load node LMA6

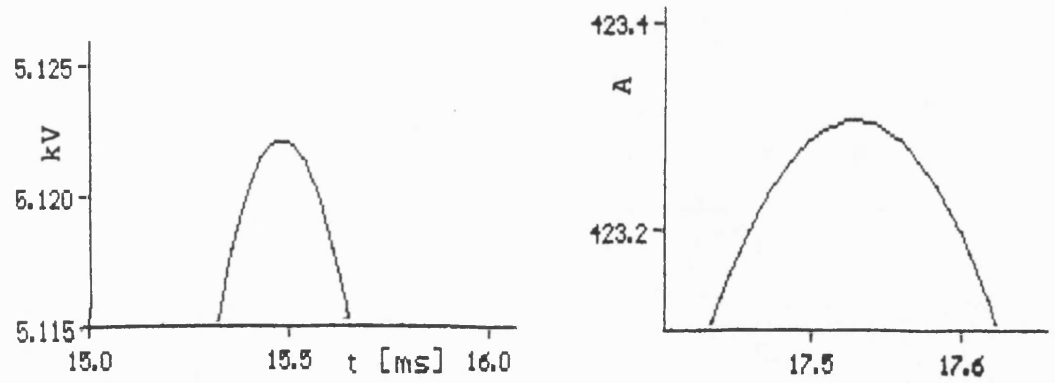


Figure 2.13

Expanded load voltage & current LMA6 at peak

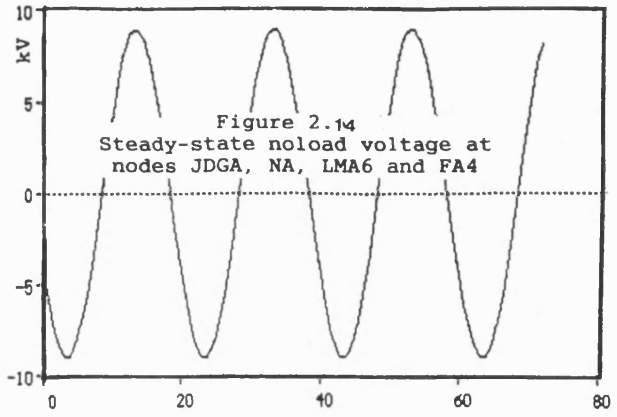


Figure 2.14
Steady-state noload voltage at nodes JDGA, NA, LMA6 and FA4

Figure 2.14
Steady-state noload voltage at nodes JDGA, NA, LMA6 and FA4

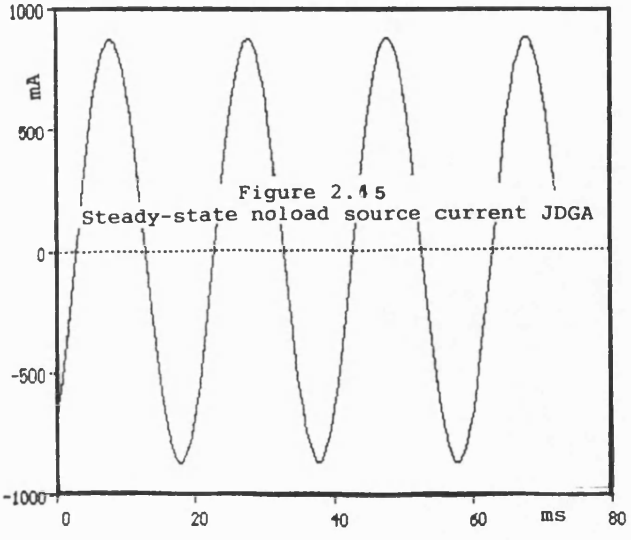


Figure 2.15
Steady-state noload source current JDGA

Figure 2.15
Steady-state noload source current JDGA

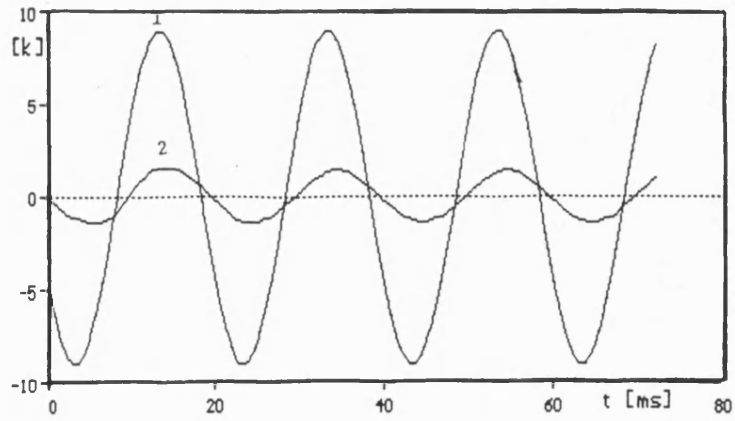


Figure 2.16
Transient voltage and current at source node JDGA
1.Source voltage at JDGA, 2.Source current at JDGA

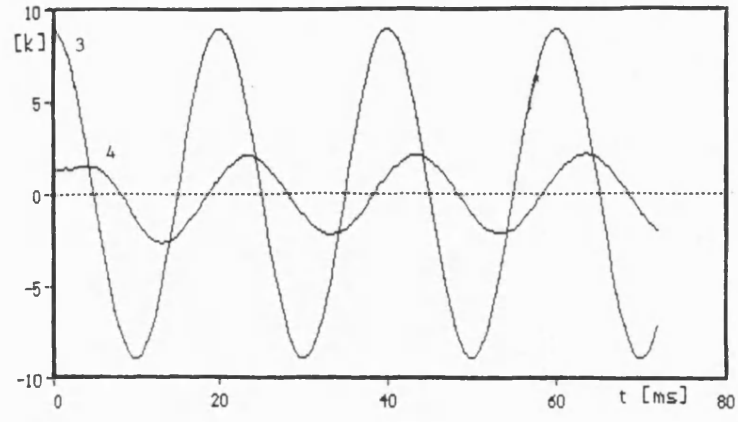


Figure 2.17
Transient voltage and current at source node JDGB
3.Source voltage at JDGB, 4.Source current at JDGB

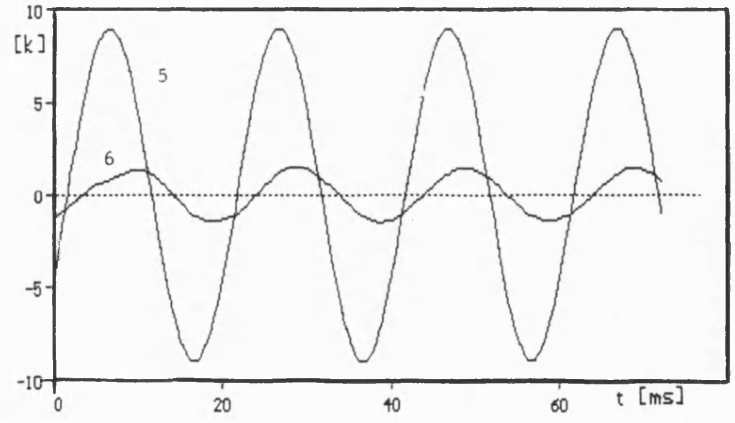


Figure 2.18
Transient voltage and current at source node JDGC
5.Source voltage at JDGC, 6.Source current at JDGC

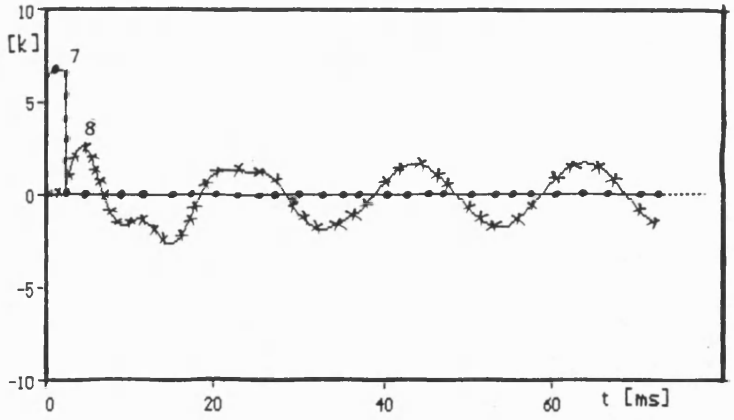


Figure 2.19
Transient voltage and current at fault node YARB
7. Node voltage YARB 8.Earth fault current YARB

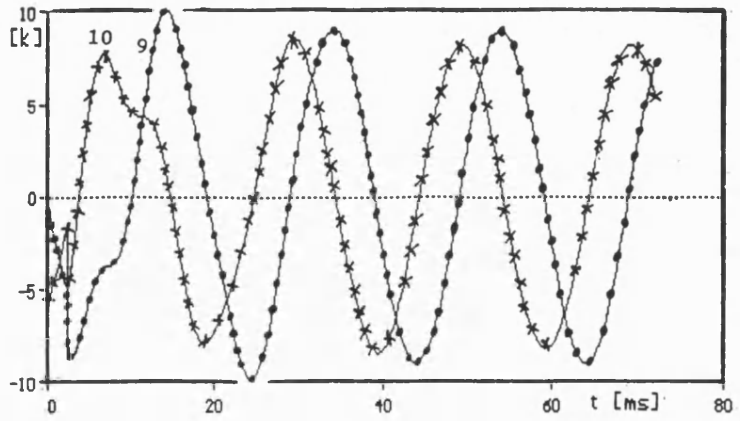


Figure 2.20
Transient voltage at nodes YARA and YARC
9.Node voltage at YARA, 10.Node voltage at YARC

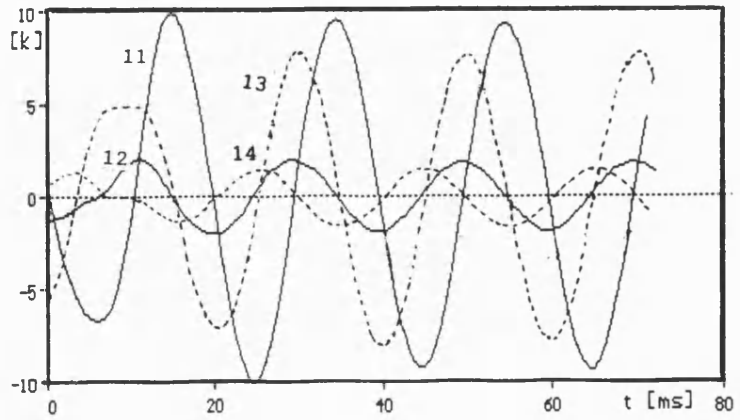


Figure 2.21
Transient voltage & capacitor current at FA2 & FC2
11.Node voltage at FA2,12.Capacitor current at FA2
13.Node voltage at FC2,14.Capacitor current at FC2

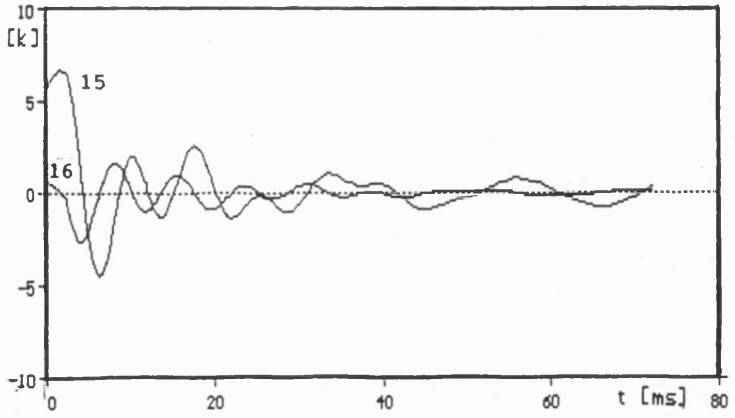


Figure 2.22
Transient voltage & capacitor current at FB2
15.Node voltage at FB2,16.Capacitor current at FB2

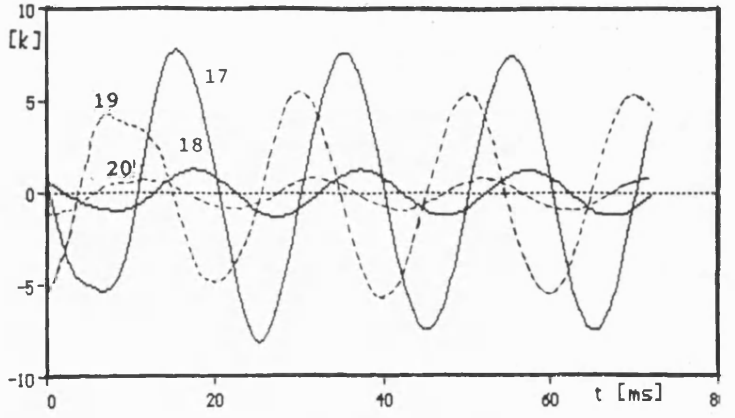


Figure 2.23
Transient load voltage and current at NA & NC
17.Load voltage at NA, 18.Load current at NA
19.Load voltage at FC, 20.Load current at FC

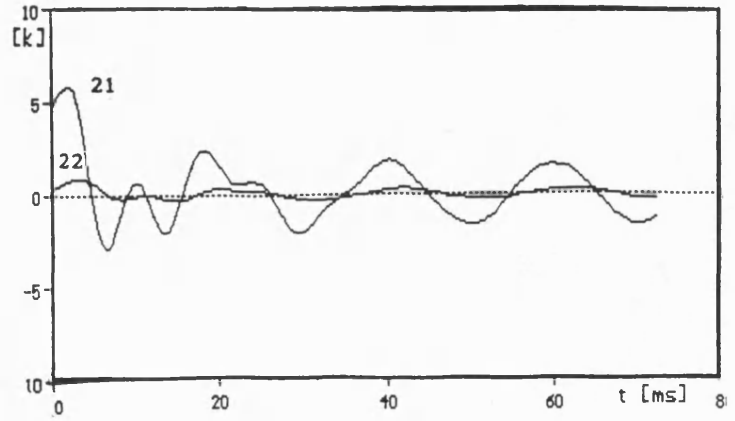


Figure 2.24
Transient load voltage and current at NB
21.Load voltage at NB, 22.Load current at NB

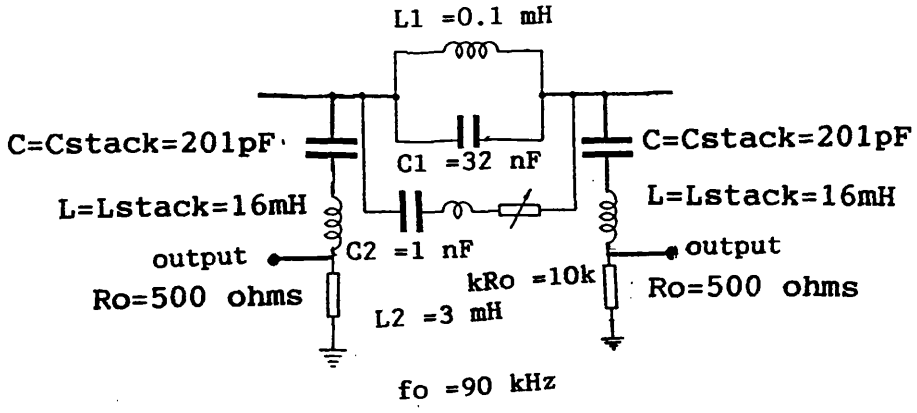


Figure 3.1, Past fault locator

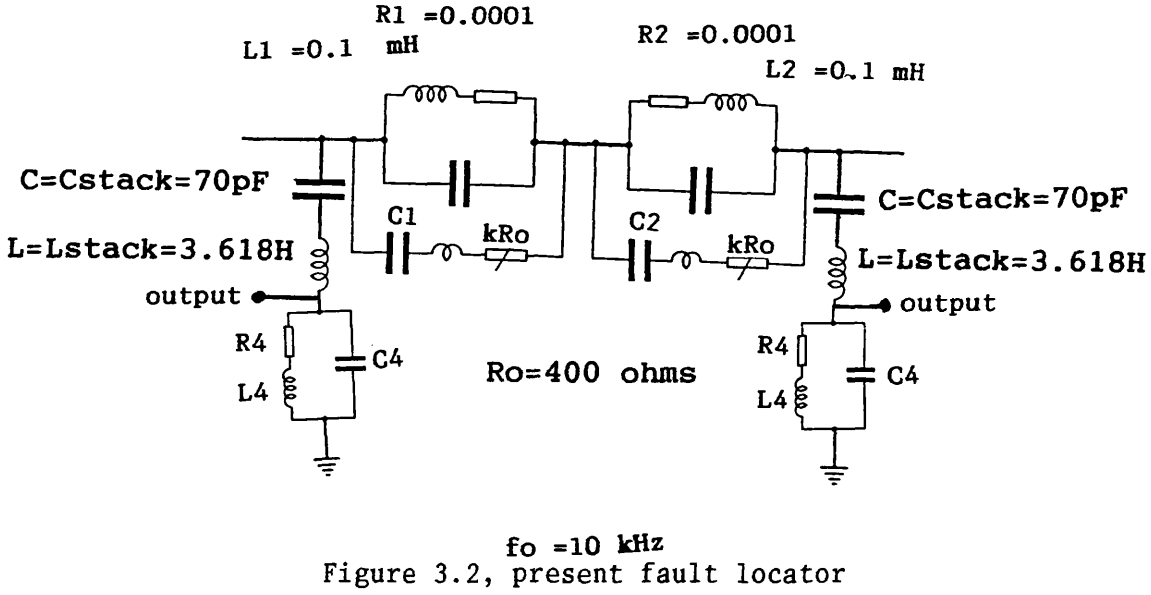


Figure 3.2, present fault locator

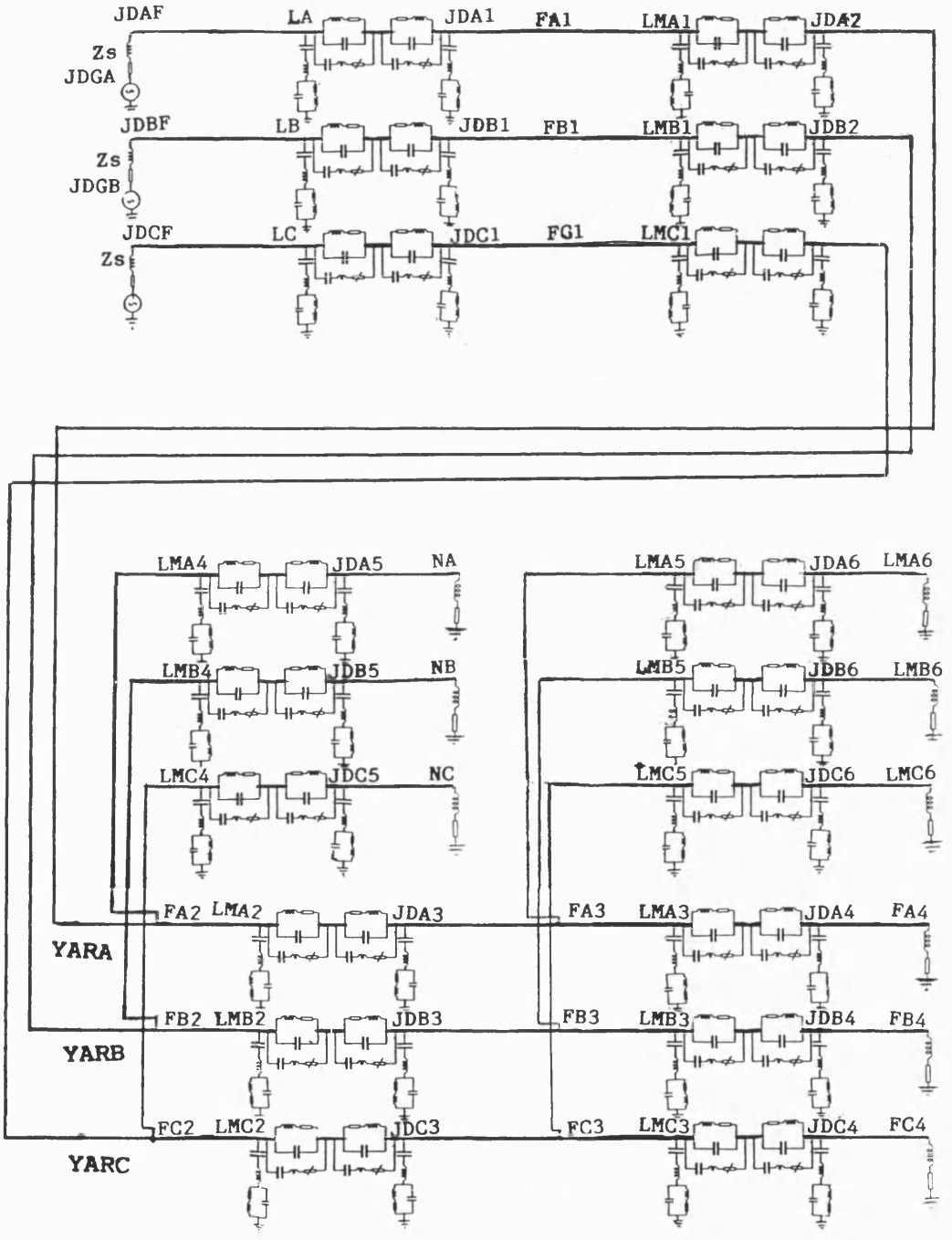


Figure 3.3 from figure 2.4 showing installation of fault locators in the distribution network.

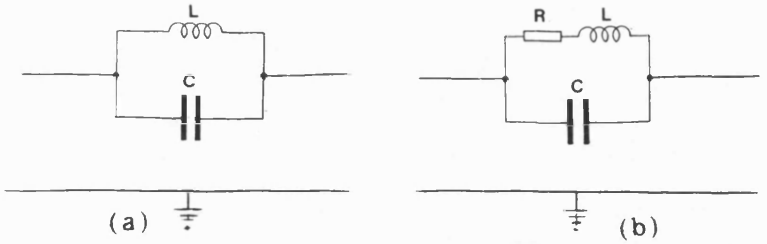


Figure 4.1
A two-branch trap for power system.

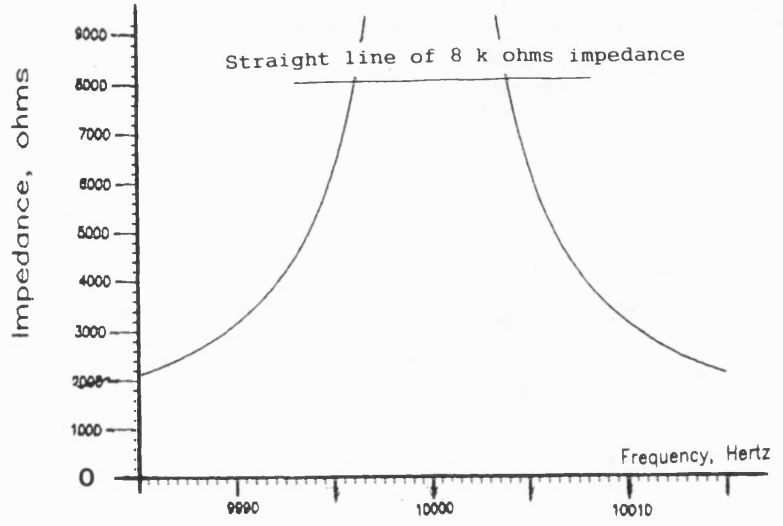


Figure 4.2
Bandwidth of a two-branch trap at 8k ohm frequencies

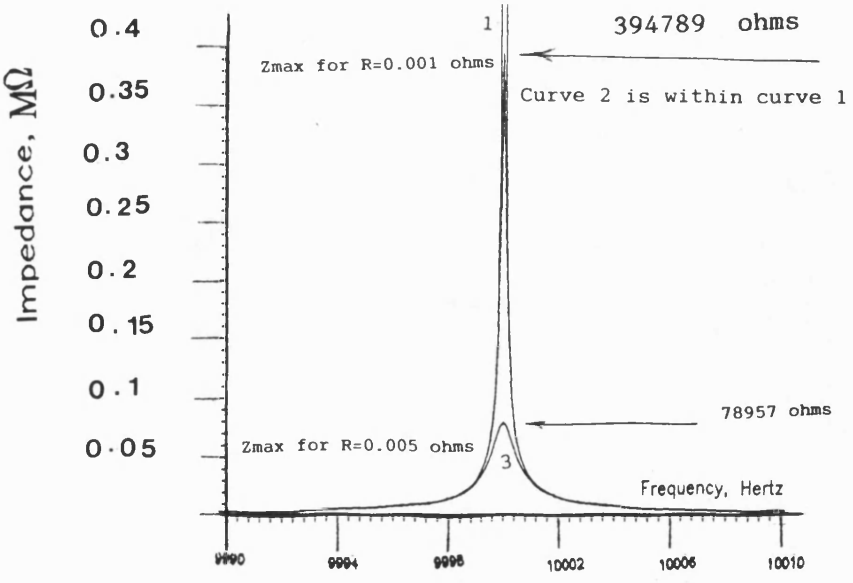


Figure 4.3
Effect of resistance on resonant impedance

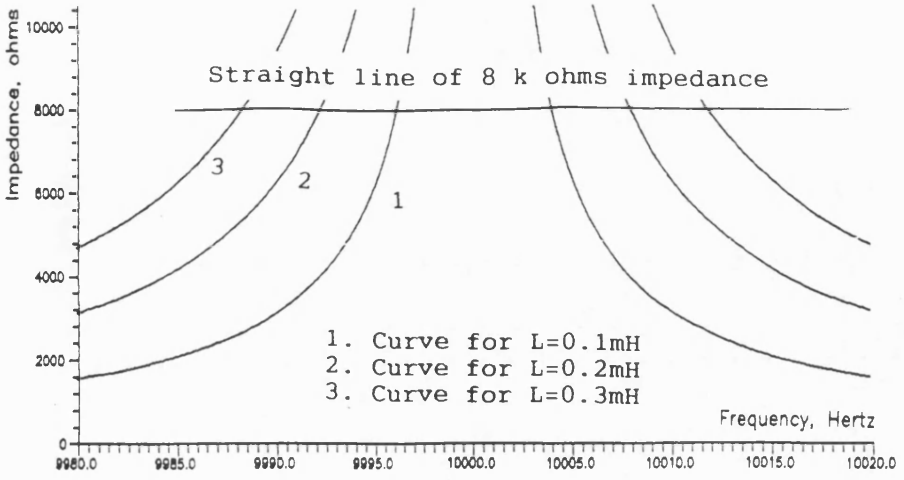


Figure 4.4
Effect of inductance on bandwidth
of a two-branch trap.

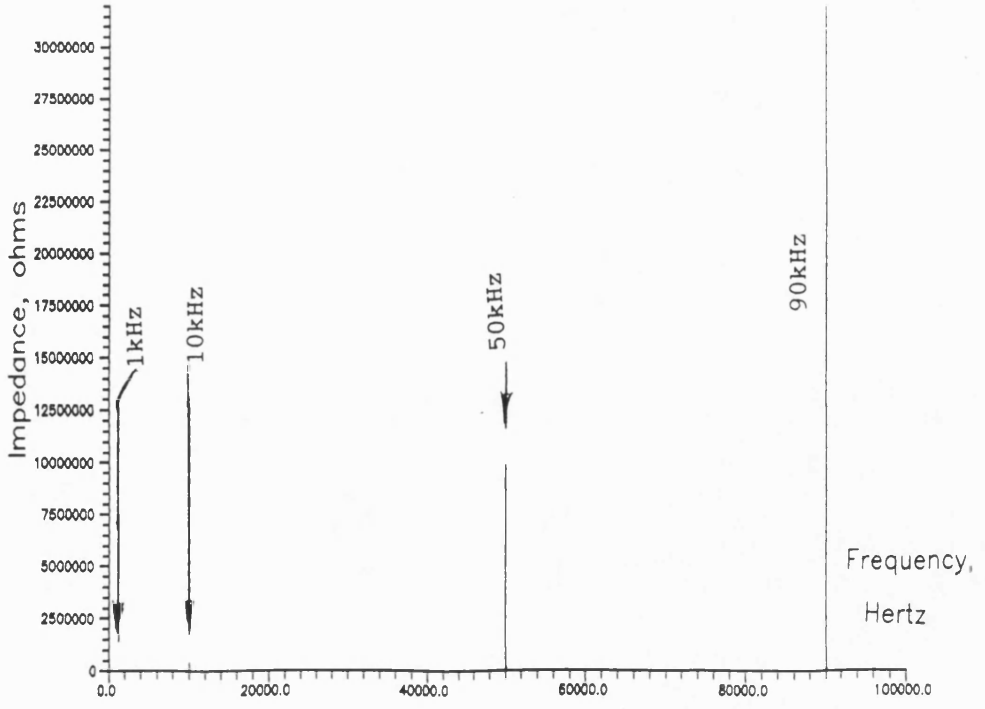


Figure 4.5
Effect of f_0 on resonant impedance of a
two-branch trap for constant L and R.

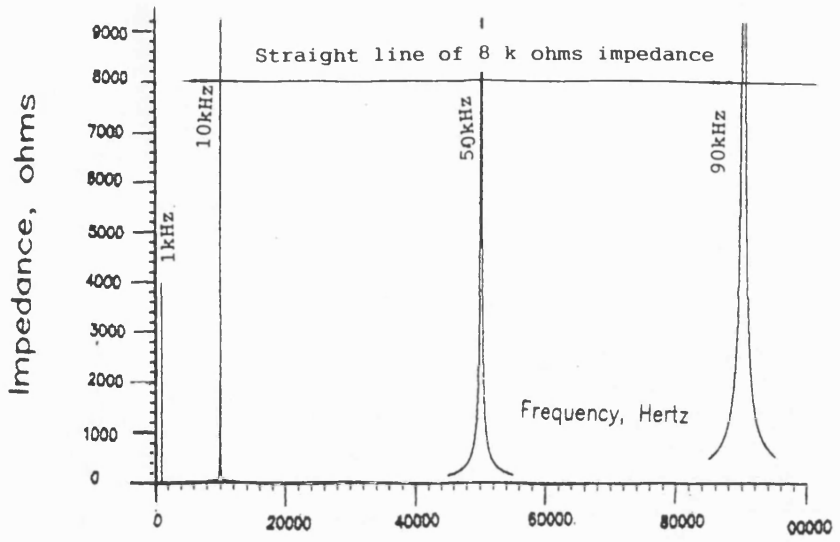


Figure 4.6
Effect of fo on bandwidth of a two-branch trap
for constant values of L and R.

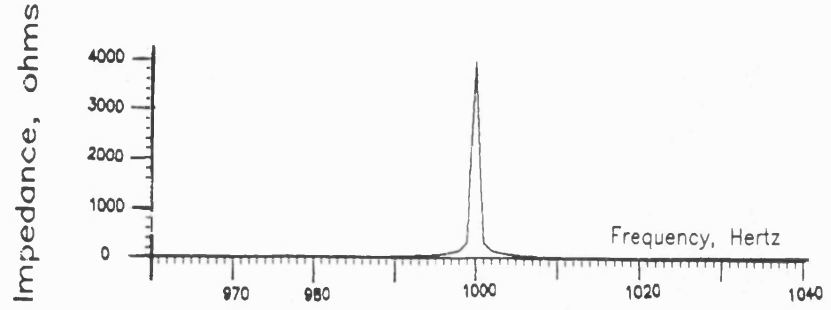


Figure 4.7
Expanded view of impedance-frequency curve of a
two-branch trap resonated at 1 kHz.

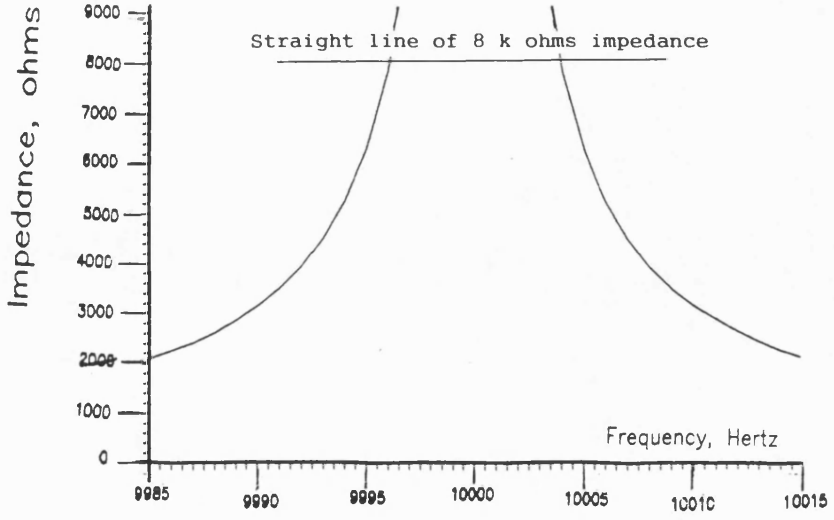


Figure 4.8
Expanded view of impedance-frequency curve of a
two-branch trap resonated at 10 kHz.

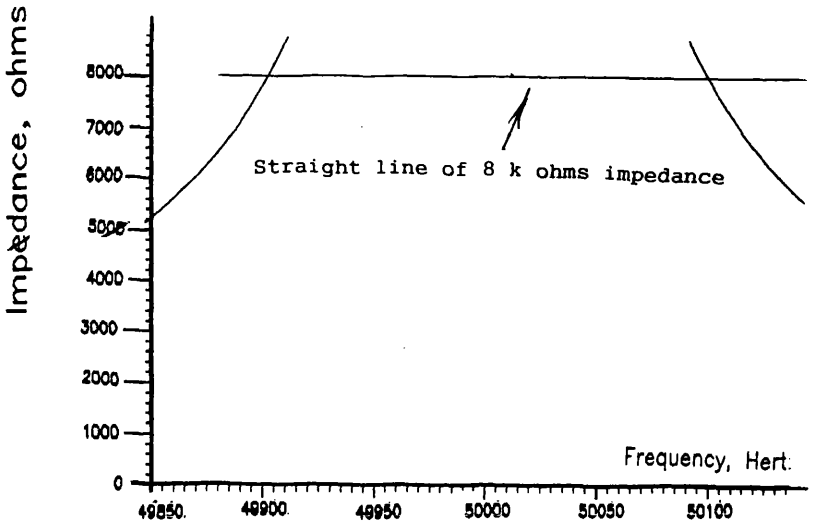


Figure 4.9
Expanded view of impedance-frequency curve of a two-branch trap resonated at 50 kHz.

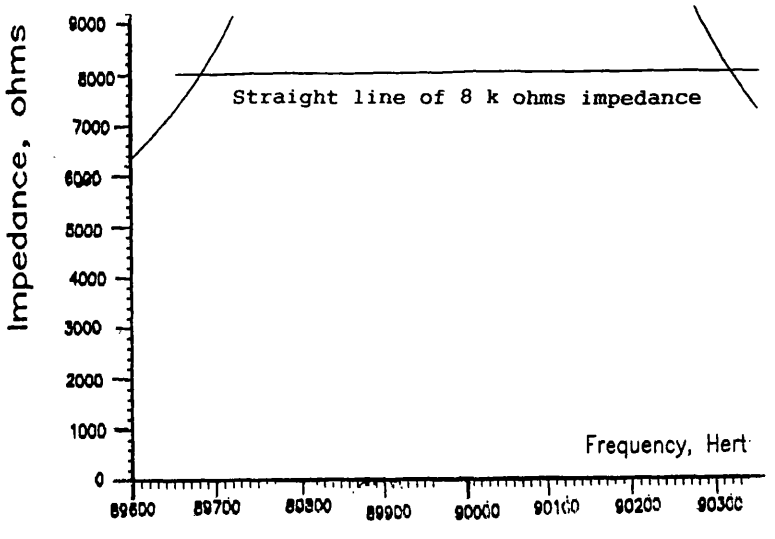


Figure 4.10
Expanded view of impedance-frequency curve of a two-branch trap resonated at 90 kHz.

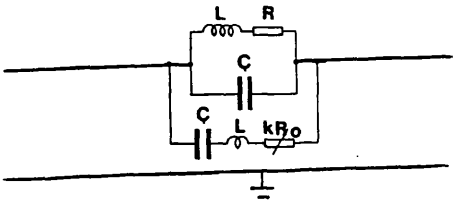


Figure 4.11
A practical wideband single trap.

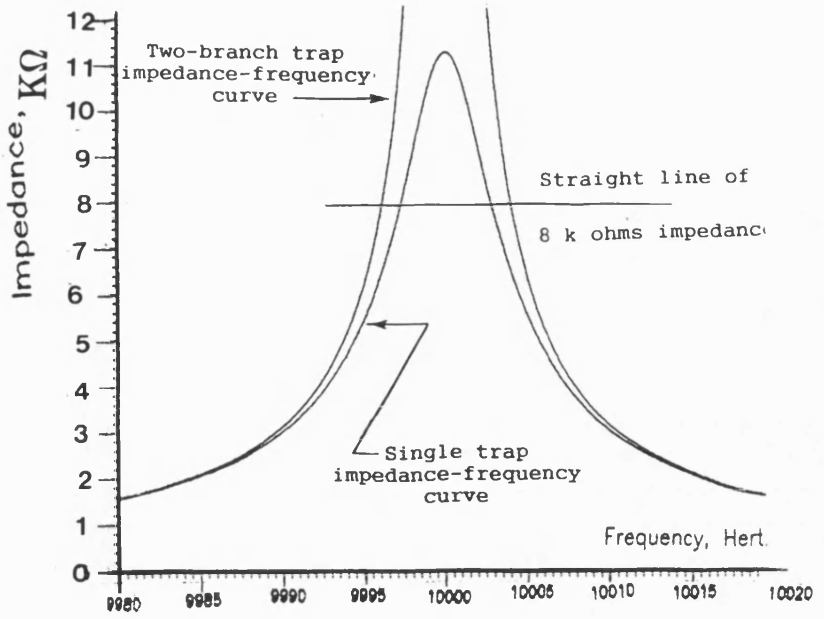


Figure 4.12
Comparision of bandwidth of single trap with two-branch trap of same L,R & C.

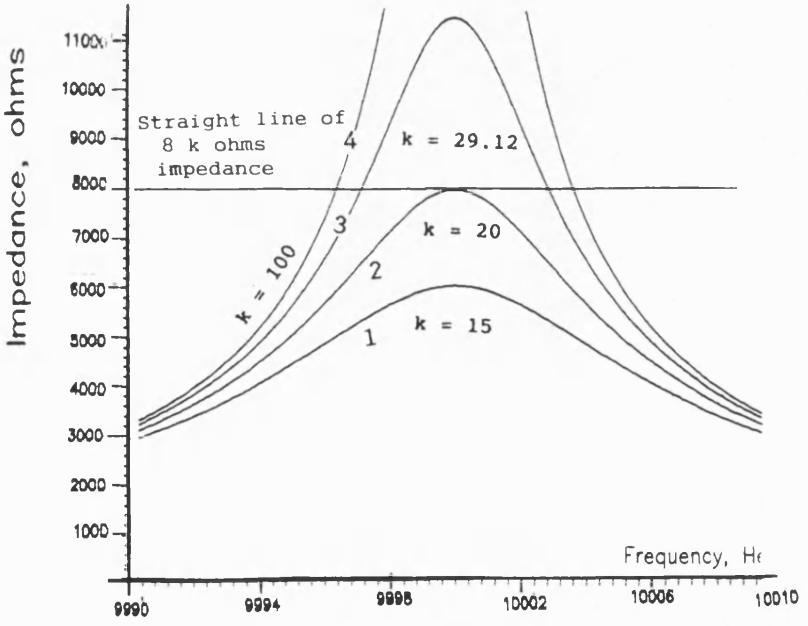


Figure 4.13
Bandwidth of a single trap for different values of k

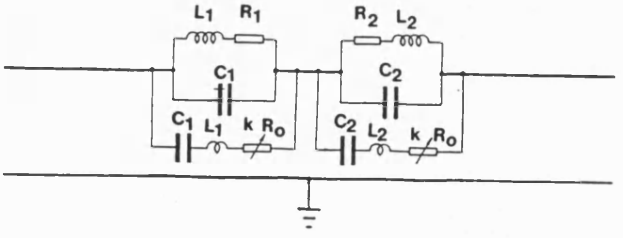


Figure 4.14
A twin trap circuit

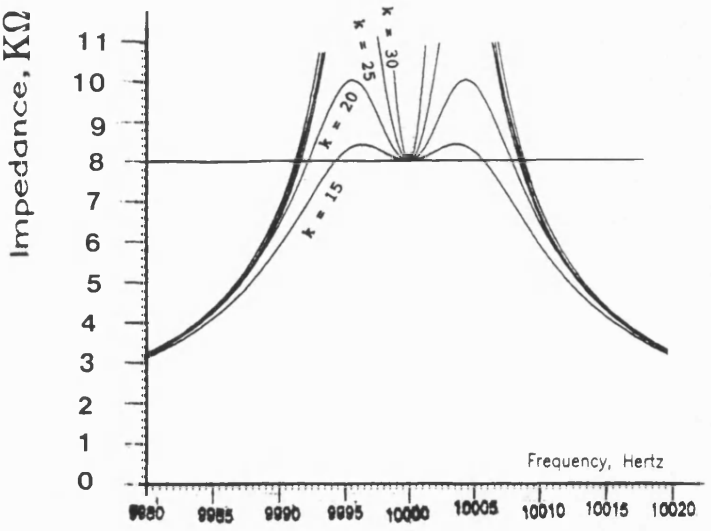


Figure 4.15
Impedance-frequency response of
twin trap for different values of k

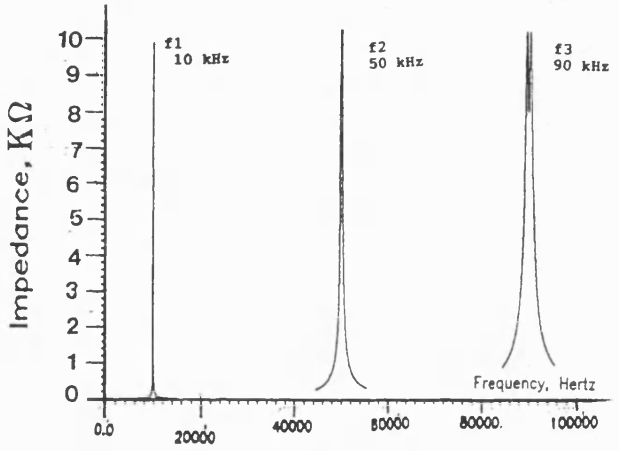


Figure 4.16
Effect of fo on bandwidth of a twin trap
for constant values of L, R, and k.

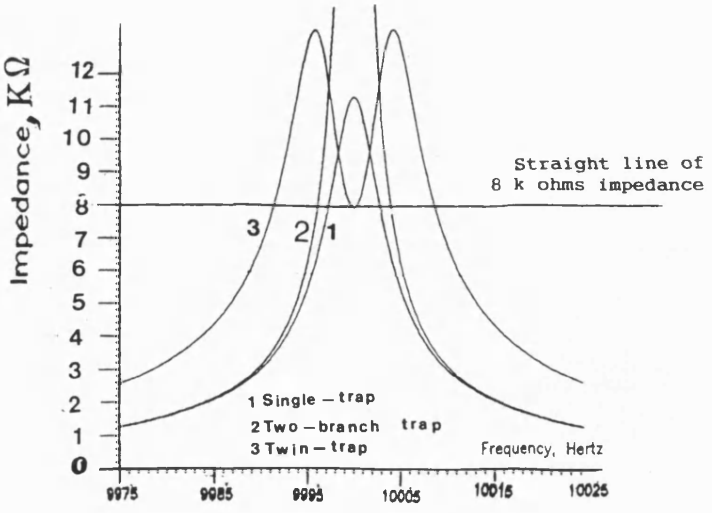


Figure 4.17
Comparision of bandwidth of a twin trap
with those of single trap and two-branch trap

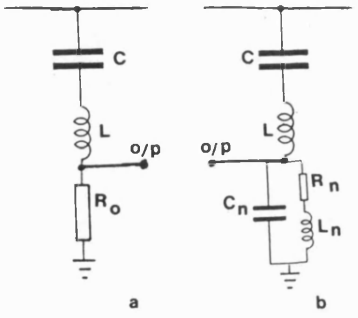


Figure 5.1
Past and present stack tuners
a) Past (series LCR) stack tuner
b) Present (series/parallel)
stack tuner

$C = C_{stack} = 70$ pF
$L = L_{stack} = 3.618$ H
$R_0 = 400$ ohms

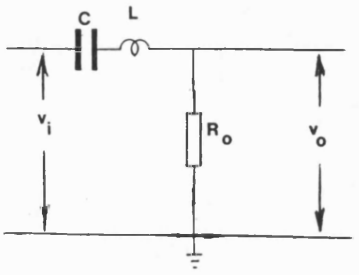


Figure 5·2
Principle of LCR circuit

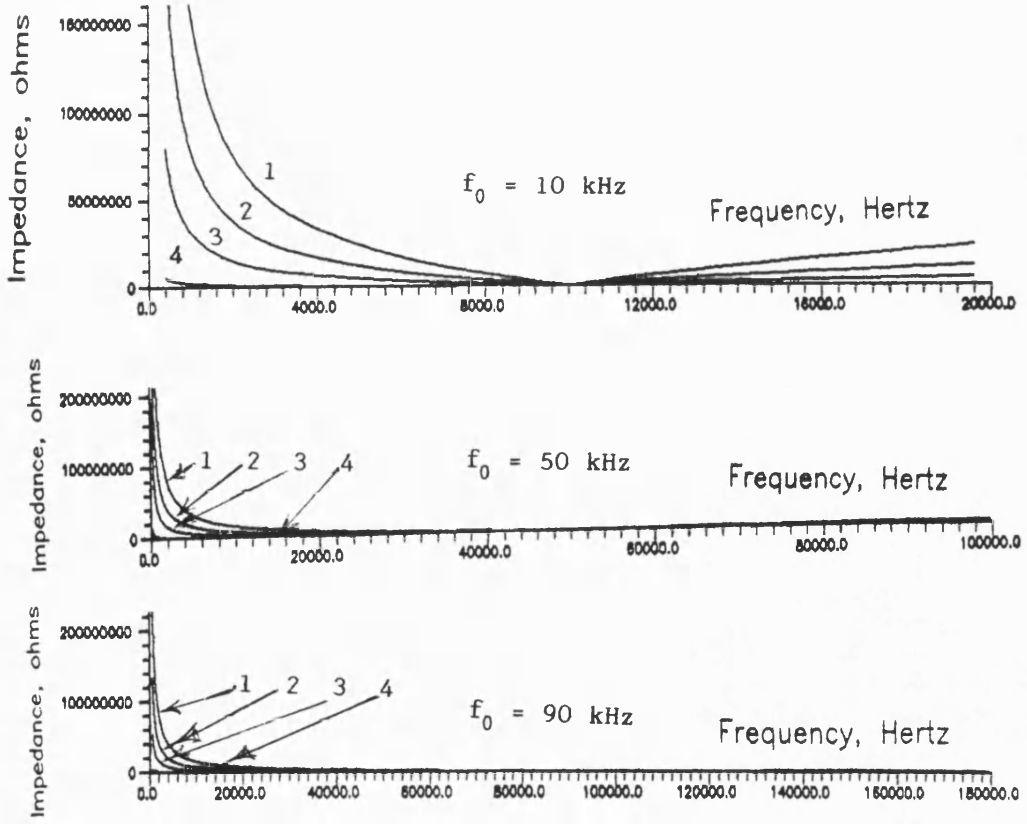


Figure 5.3
Impedance-frequency response of series stack tuners for
1.Cstack=1pF, 2.Cstack=2pF 3.Cstack=5pF & 4.Cstack=70pF

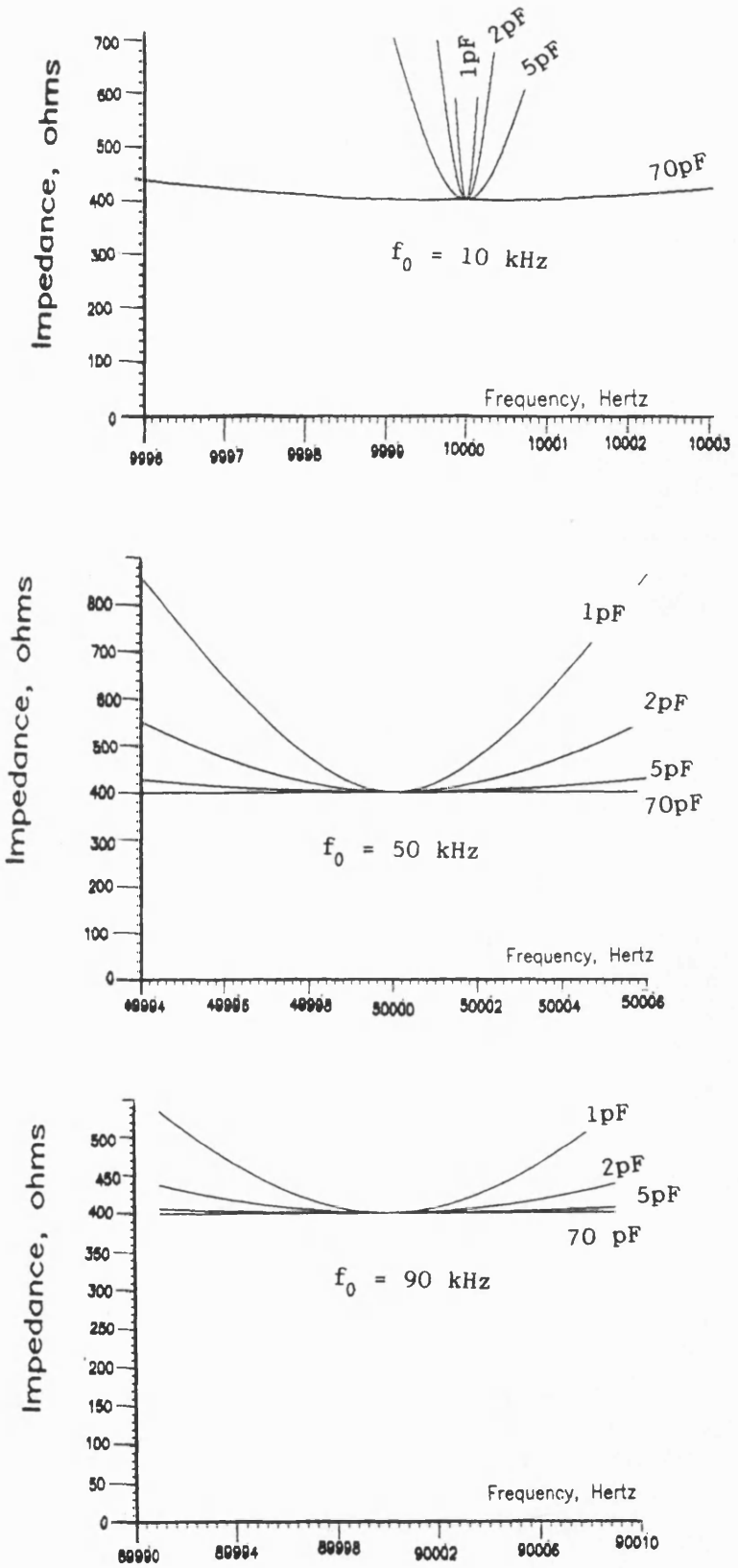


Figure 5.4
Expanded view of impedance frequency response

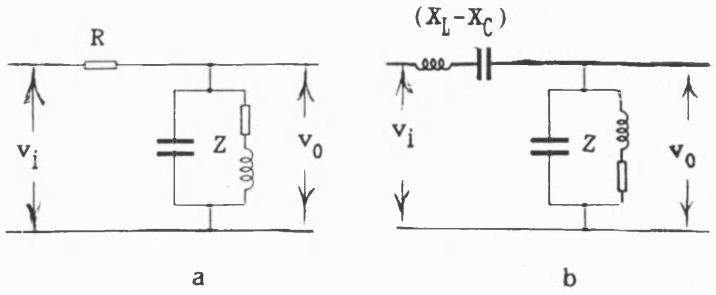


Figure 5.5
Principle of parallel resonant filter

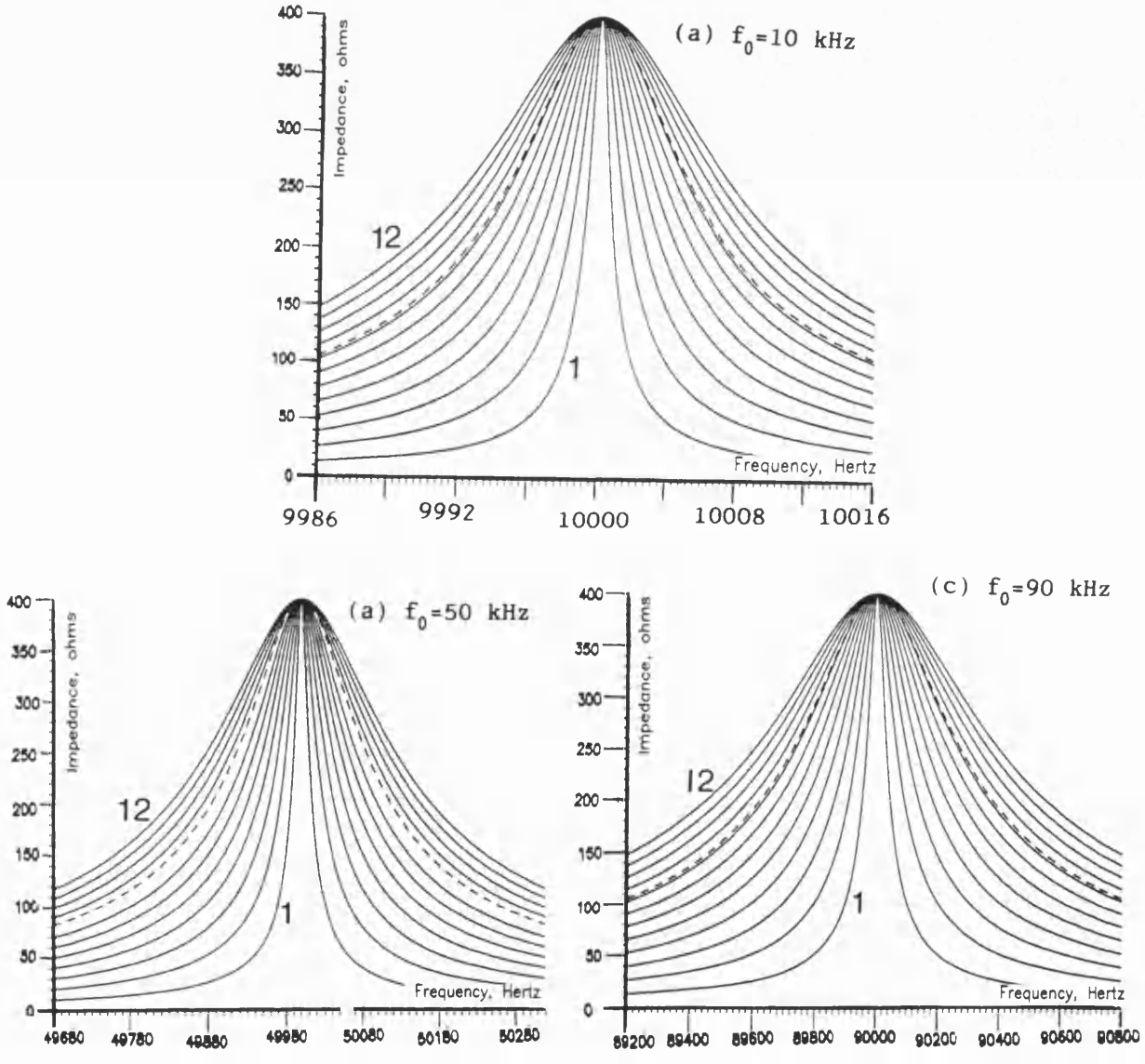


Figure 5.6
Comparison of impedance-frequency characteristic of parallel resonant circuit with that of the single-trap circuit.

- - - - trap curve
_____ parallel stack tuner

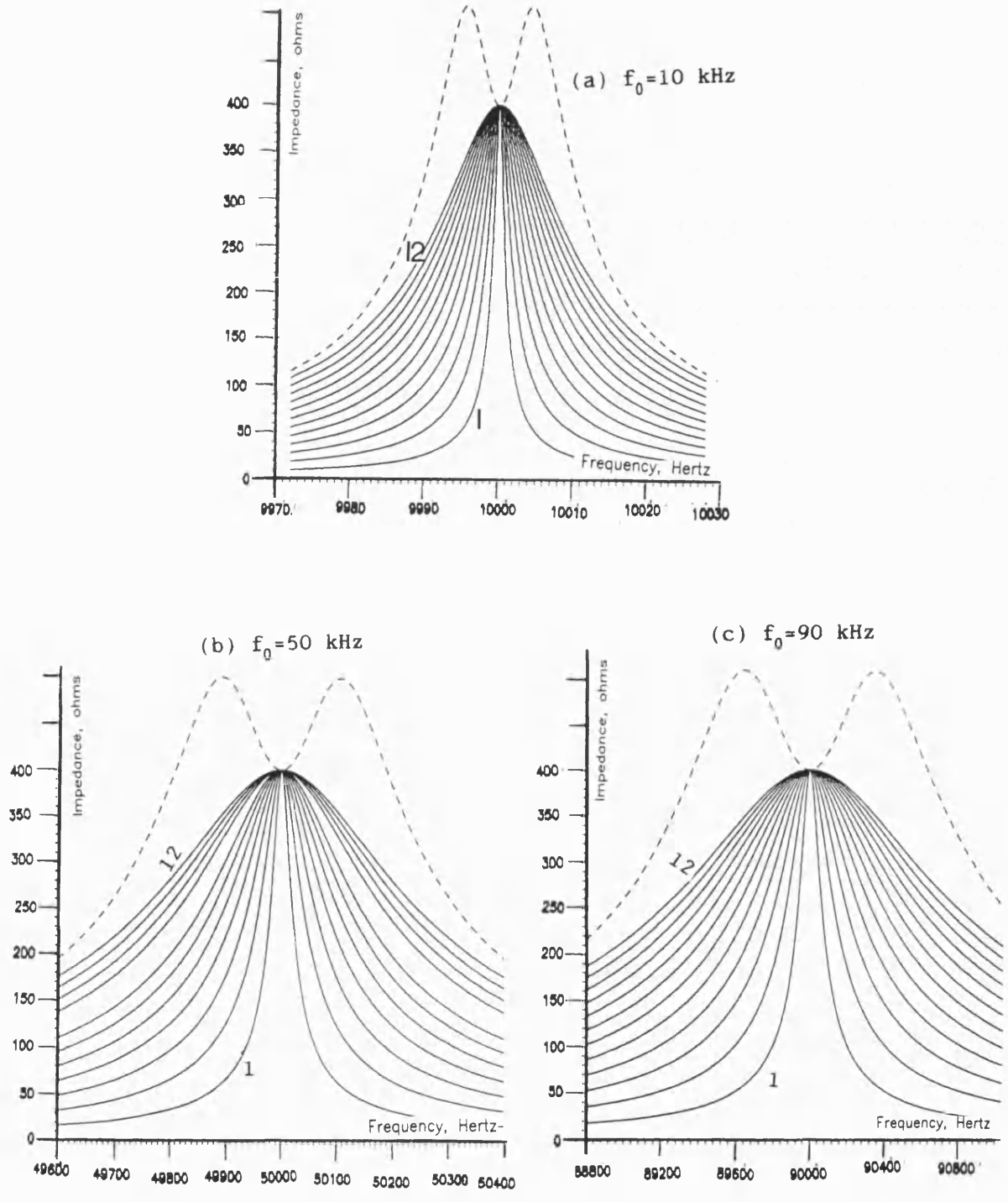


Figure 5.7
Comparison of impedance-frequency characteristics of parallel resonant circuit and twin-trap circuit

- - - - trap curve
_____ parallel stack tuner

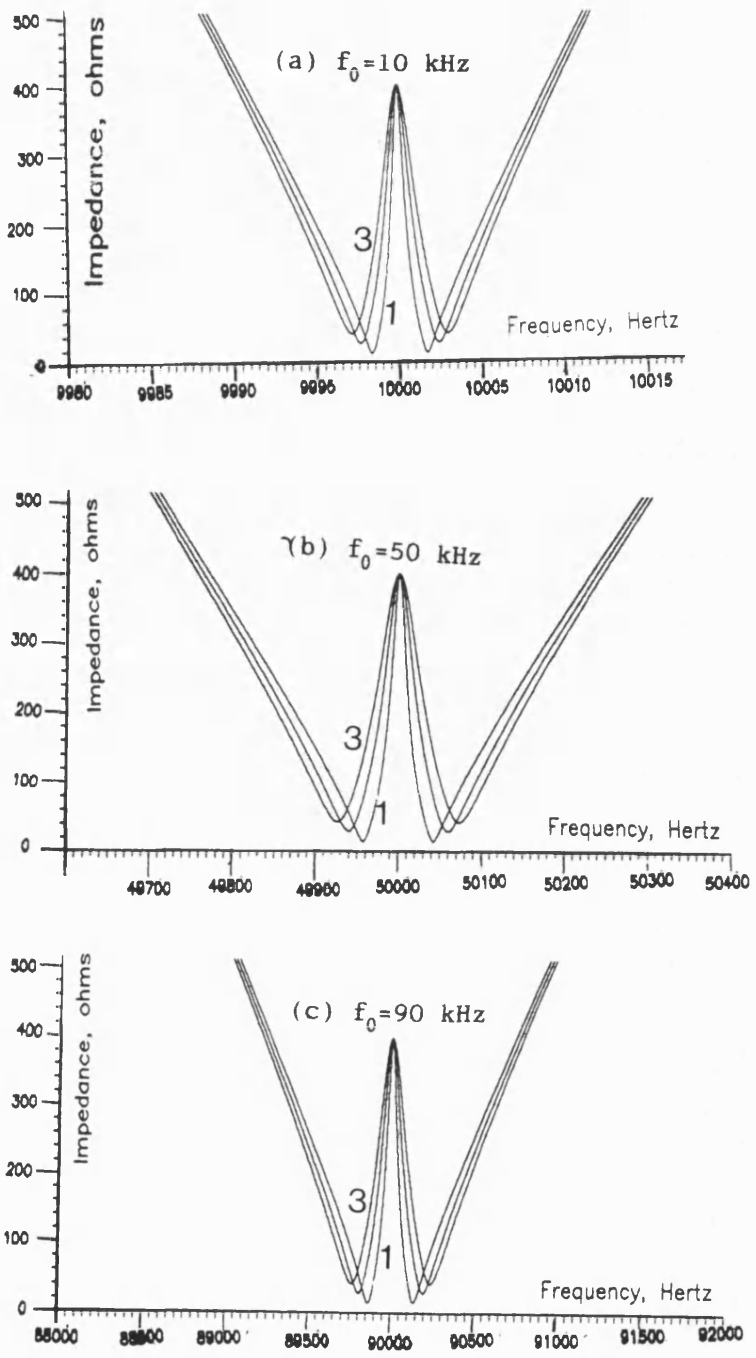


Figure 5.8
Total impedance-frequency response of series/parallel stack tuner of the single trap fault-locators for 3 different values of L_n

1. L_n=0.002083 mH 2. L_n=0.0025 mH 3. L_n=0.002917 mH

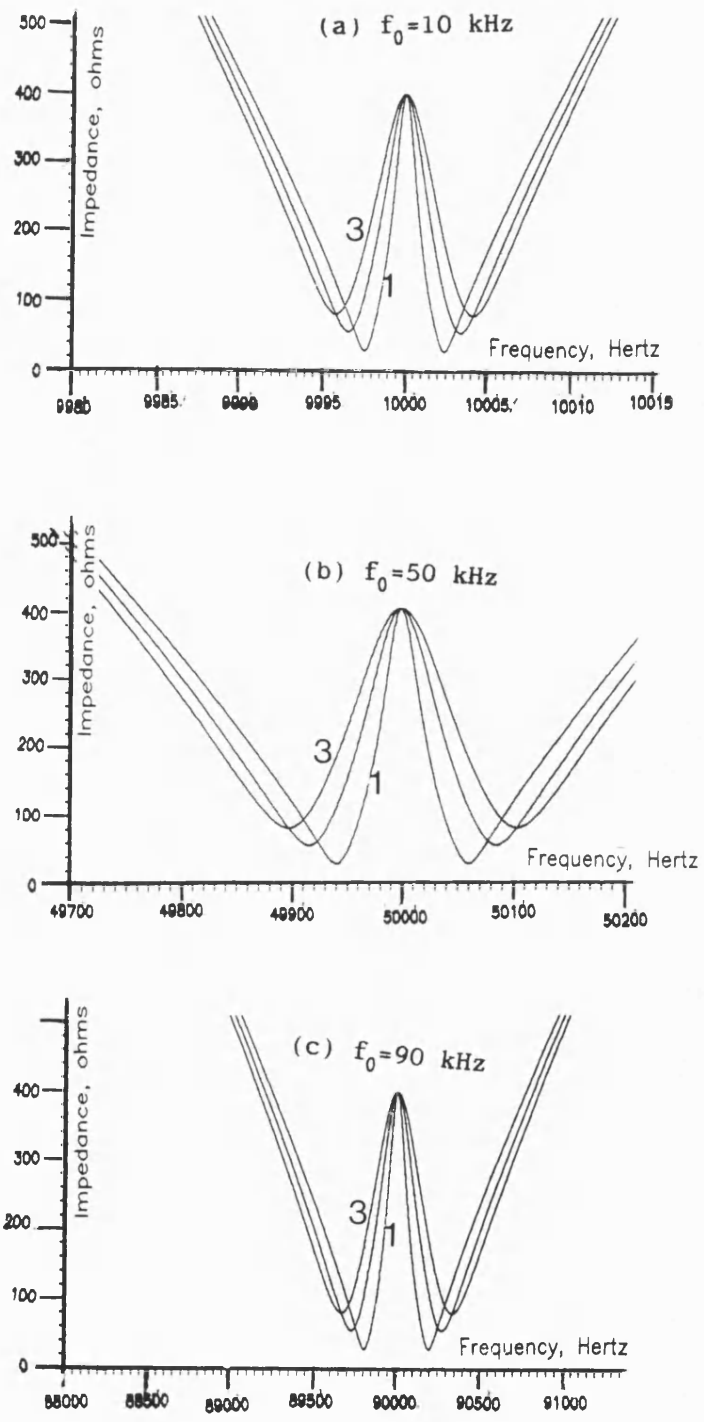


Figure 5.9
Total impedance-frequency response of series/parallel stack tuner of the twin trap fault-locators for 3 different values of L_n

1. L_n=0.00417 mH 2. L_n=0.005 mH 3. L_n=0.005833 mH

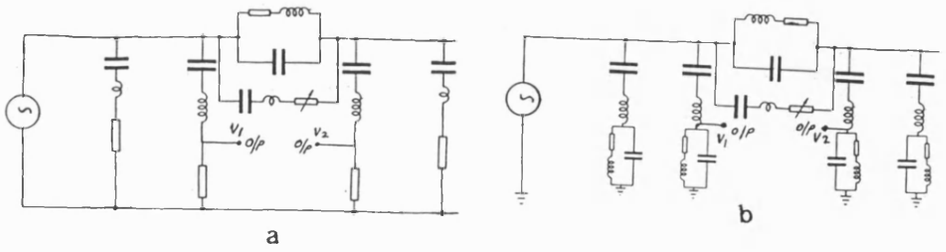


Figure 6.1
Circuit arrangement to study frequency-response of fault locator
a)with series LCR stack tuner,b)with series/parallel stack tuner

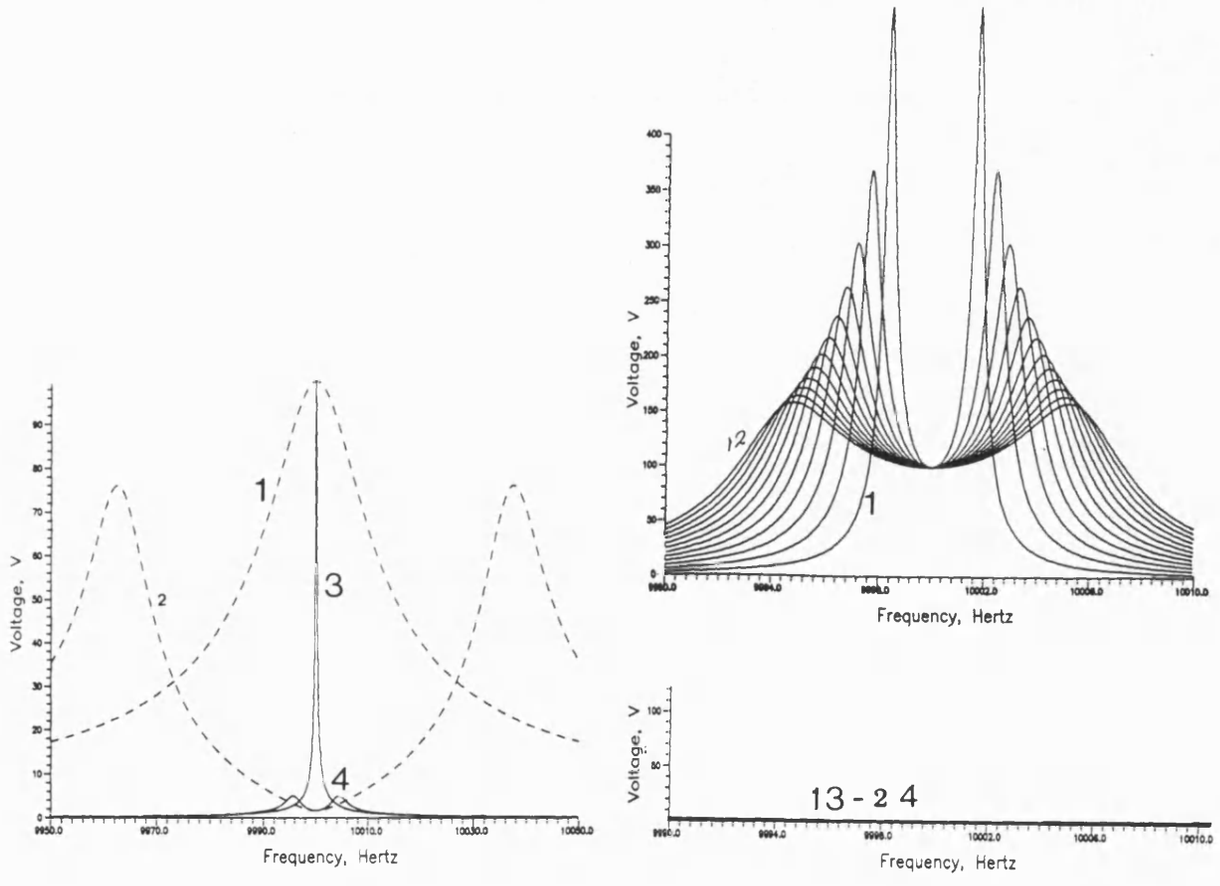


Figure 6.2
Output-voltage versus frequency response
for constant input voltage of 100 volts.
1) 70pF,series stack tuner close to Fault
2) 70pF,series stack tuner away from fault
3) 1pF, series stack tuner close to fault
4) 1pF, series stack tuner away from fault

- - - - C_{stack} = 70 pF
_____ C_{stack} = 1 pF

Figure 6.3
Output-voltage versus frequency response
for constant input voltage of 100 volts
for 12 different values of L_n
(1-12) stack tuner close to Fault
(13-24 stack tuner away from fault

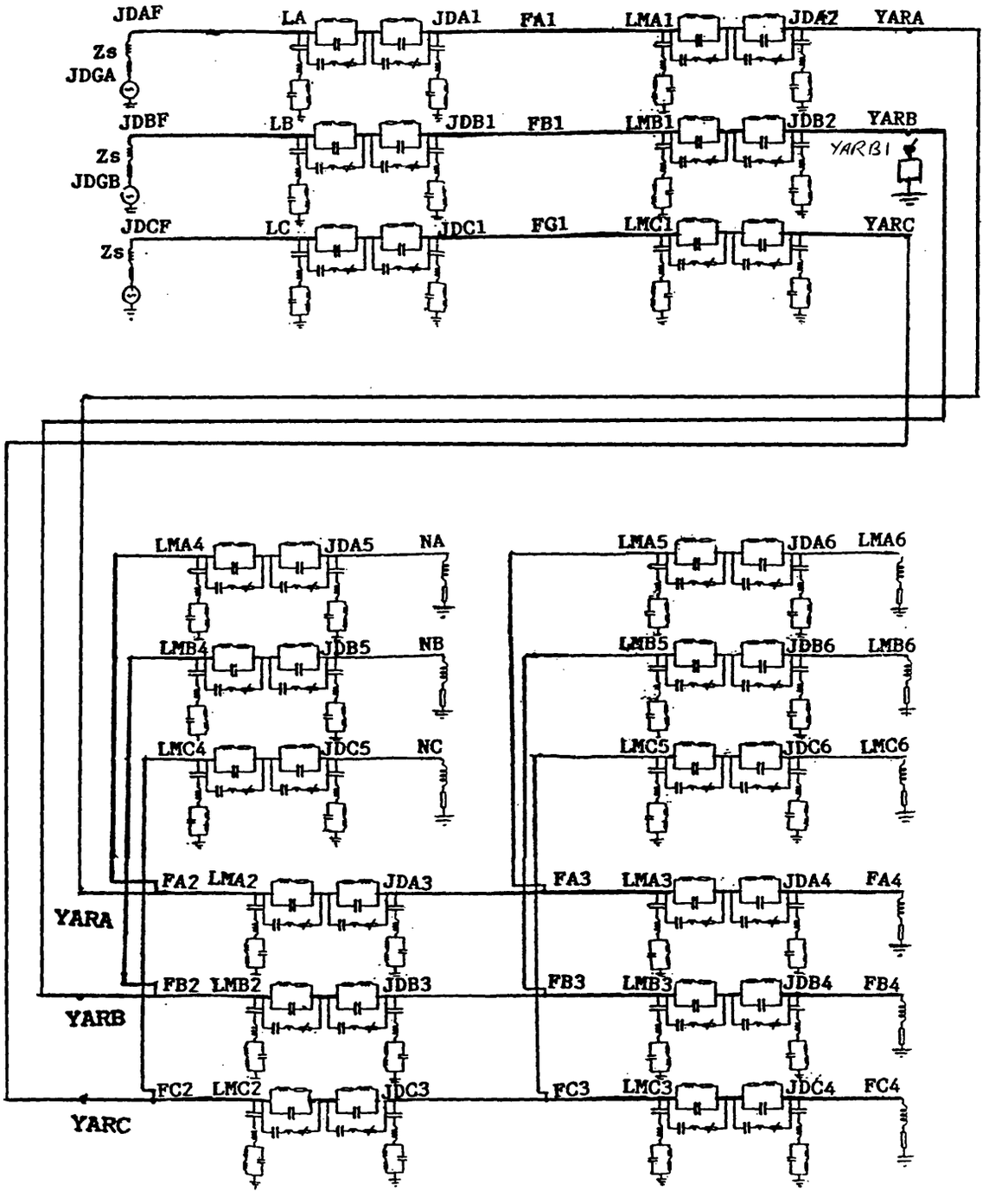


Figure 7.1
Three-phase distribution network to study parameter related performance of fault locator

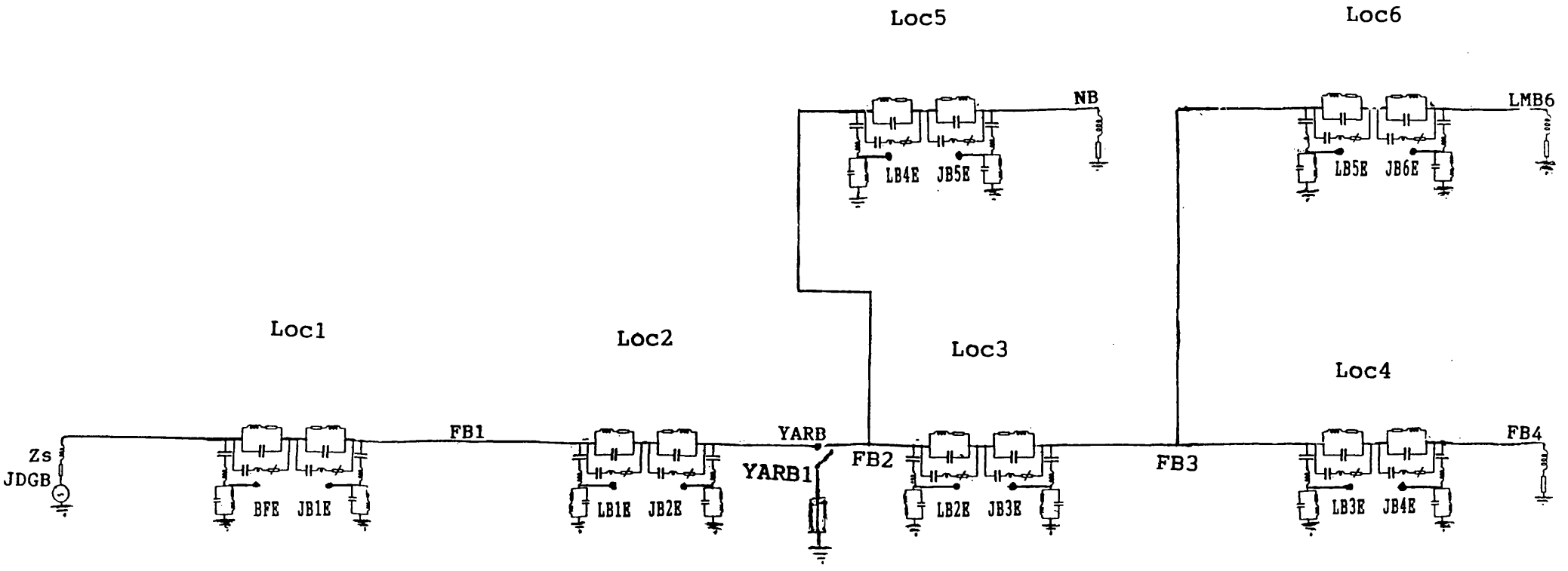


Figure 7.2
Phase-B single line diagram showing installation
and output terminals of fault locators

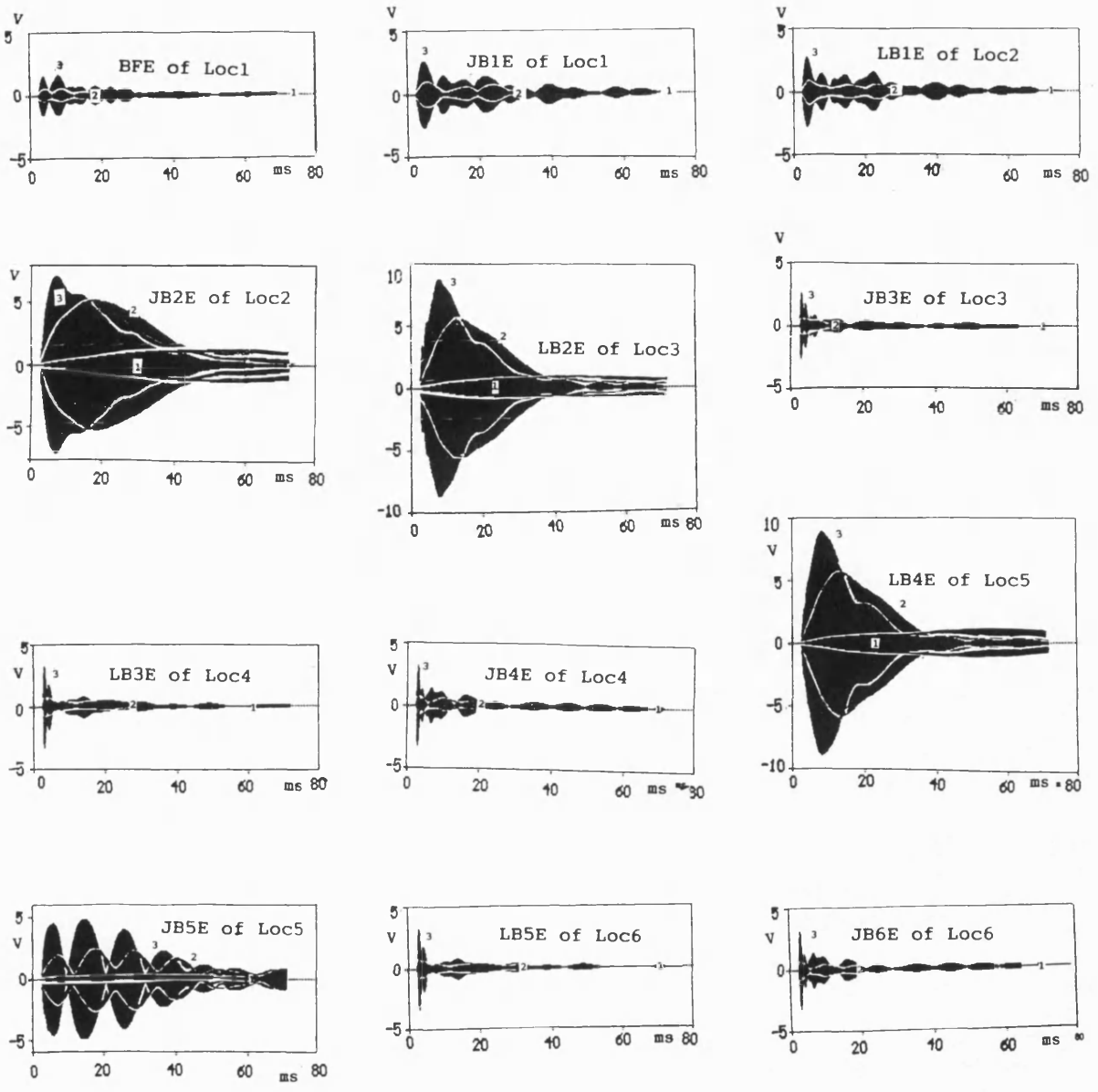


Figure 7.3a (Loaded system)
Signal output voltages from stack tuners using (1) L_n =0.001mH, (2) L_n =0.02mH and (3) L_n =0.1 mH

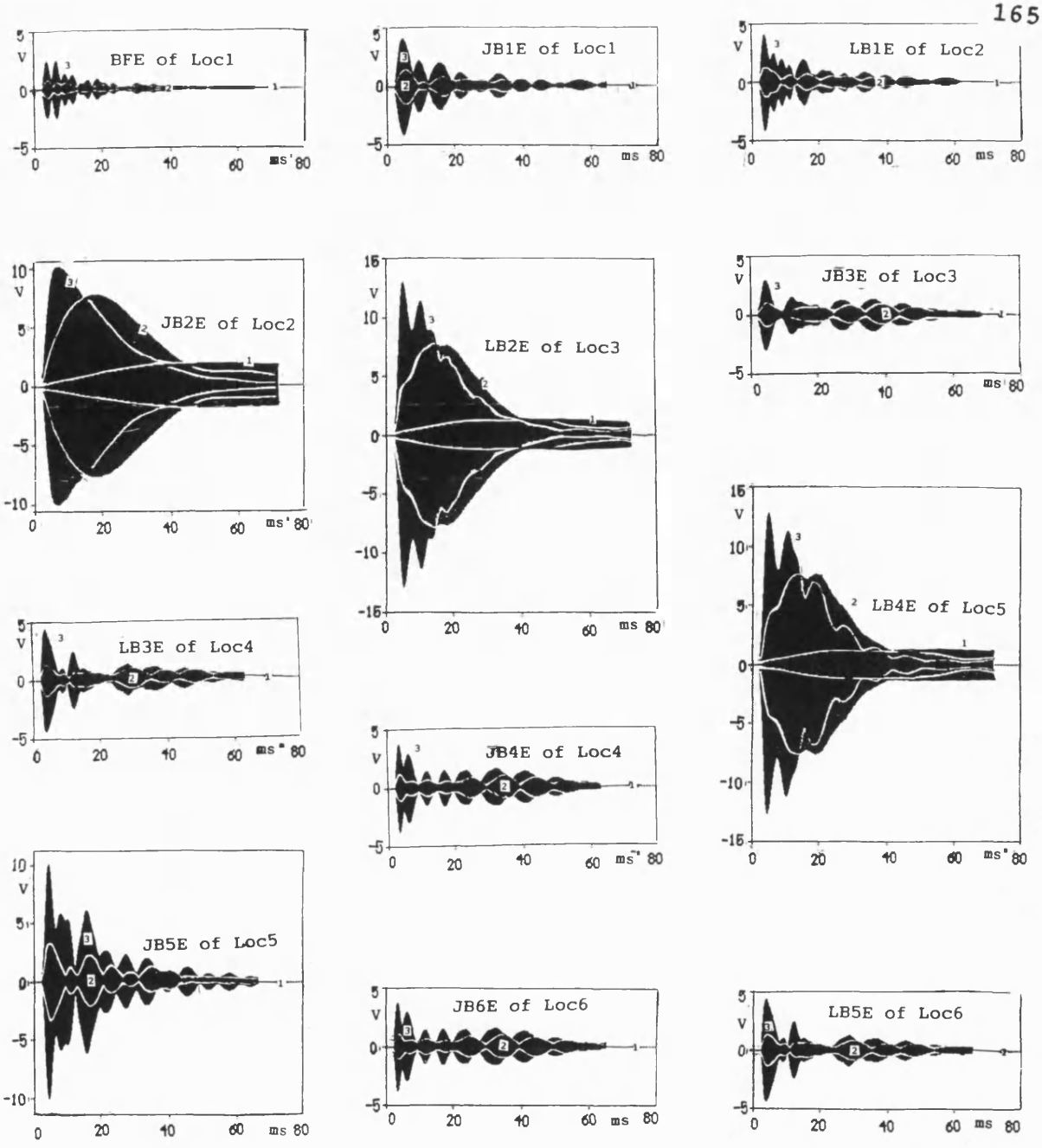


Figure 7.3b (unLoaded system)
Signal output voltages from stack tuners using (1) L_n =0.001mH, (2) L_n =0.02mH and (3) L_n =0.1 mH

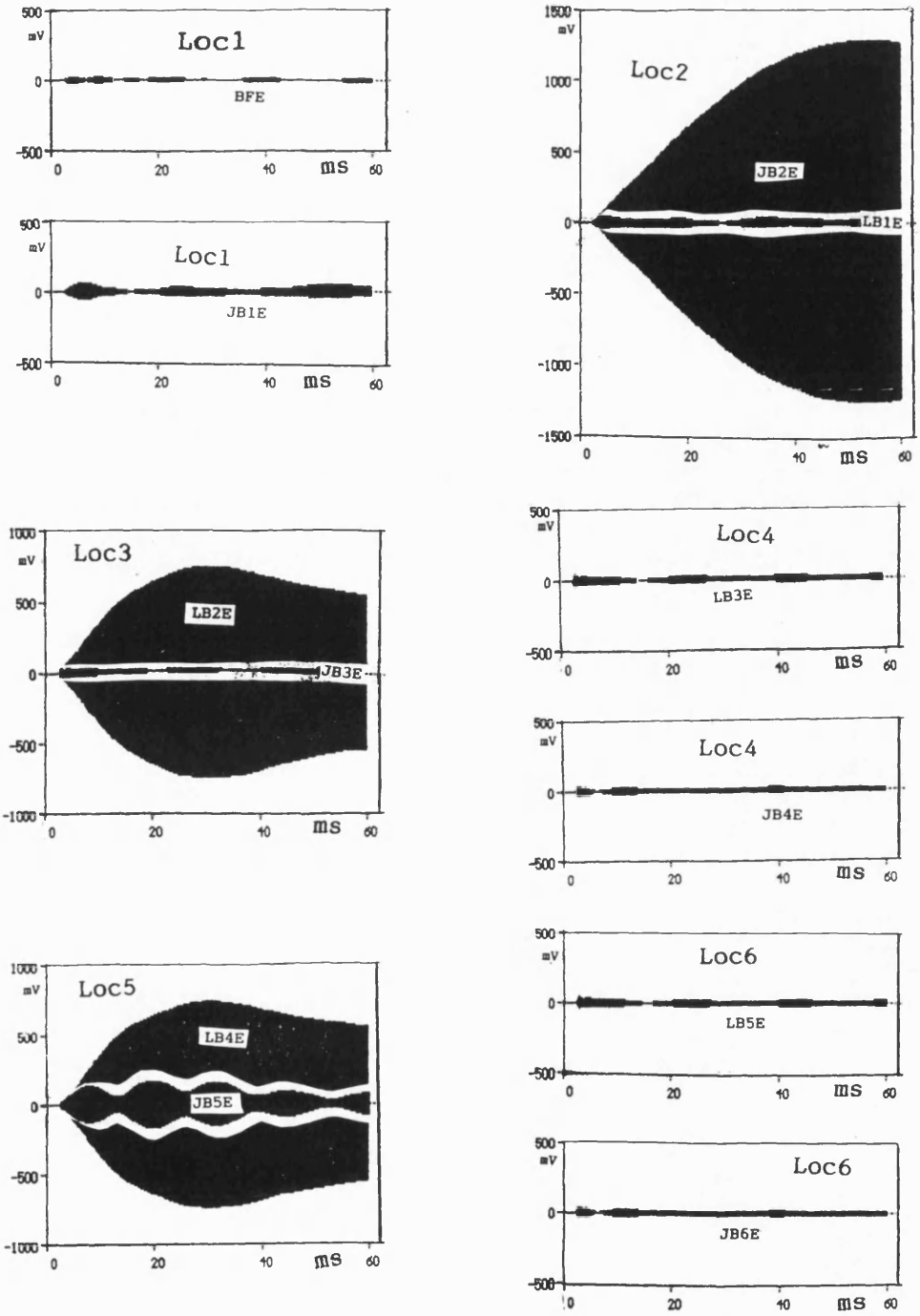


Figure 7.4a
Comparison of output signal voltages from two sides of fault locators when the system supplies normal loads. The value of L_n is 0.001mH.

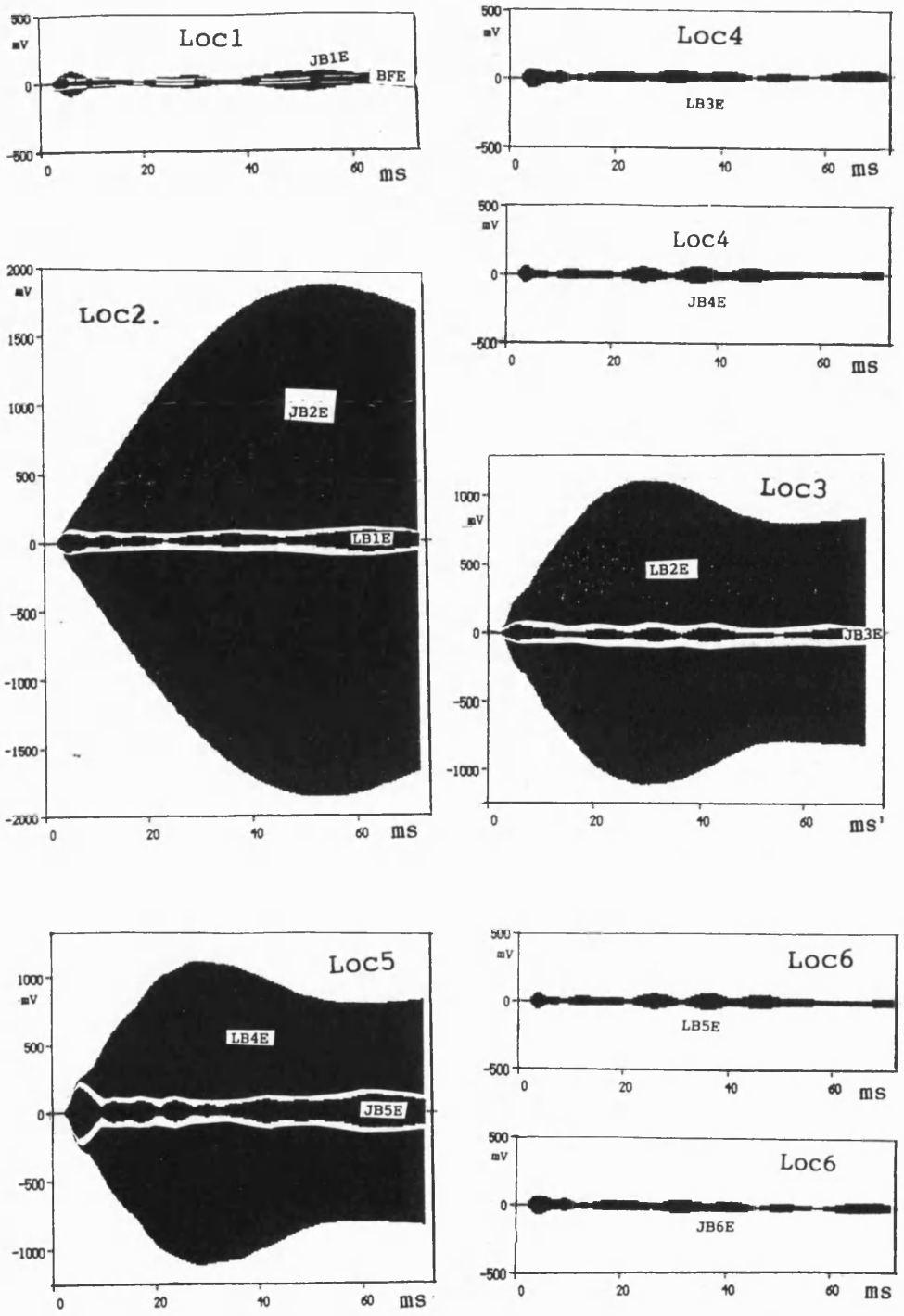


Figure 7.4b
Comparison of output signal voltages from two sides of fault locators when the system supplies no load. The value of L_n is 0.001 mH.

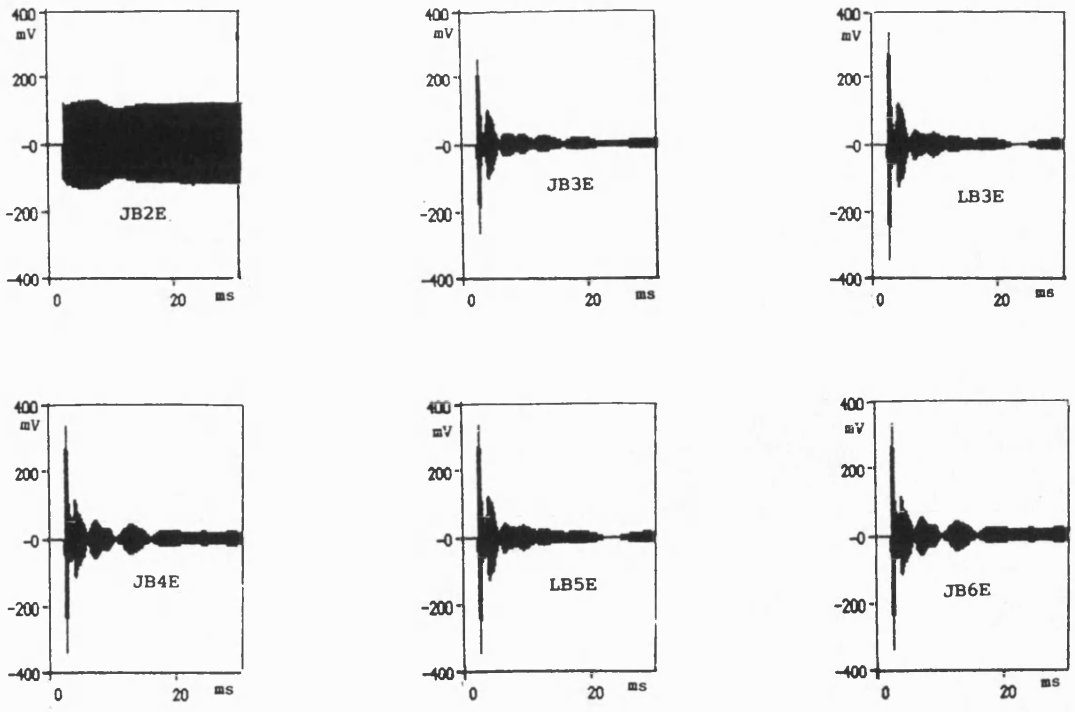


Figure 7.5 a
Comparison of output voltages from different LCR stack tuners, C_{stack} =1pF with load on terminals of the 11 kV system.

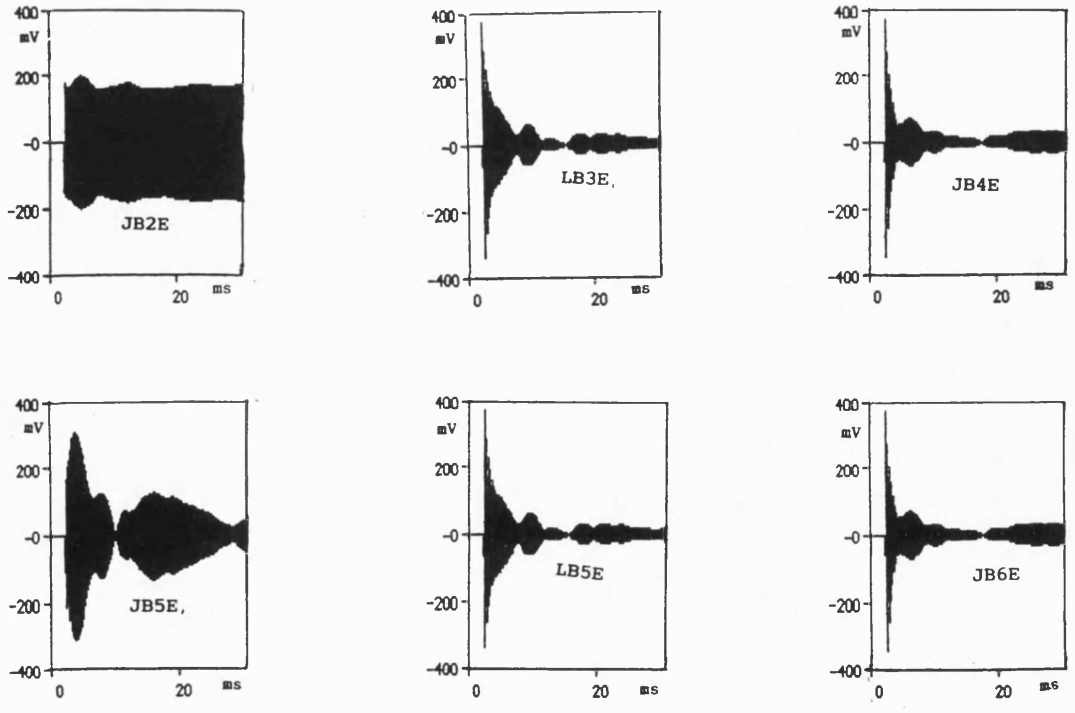


Figure 7.5 b
Comparison of output voltages from different LCR stack tuners, C_{stack} =1pF without load on terminals of the 11 kV system.

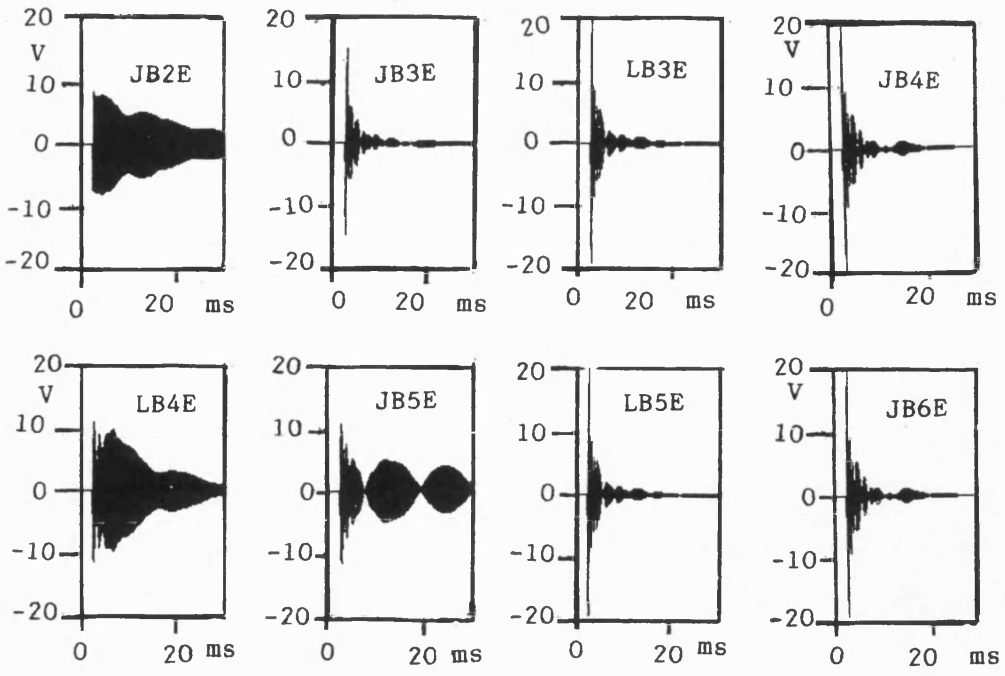


Figure 7.6 a
Comparison of output voltages from different LCR stack tuners, C_{stack} =70pF with load on terminals of the 11 kV system.

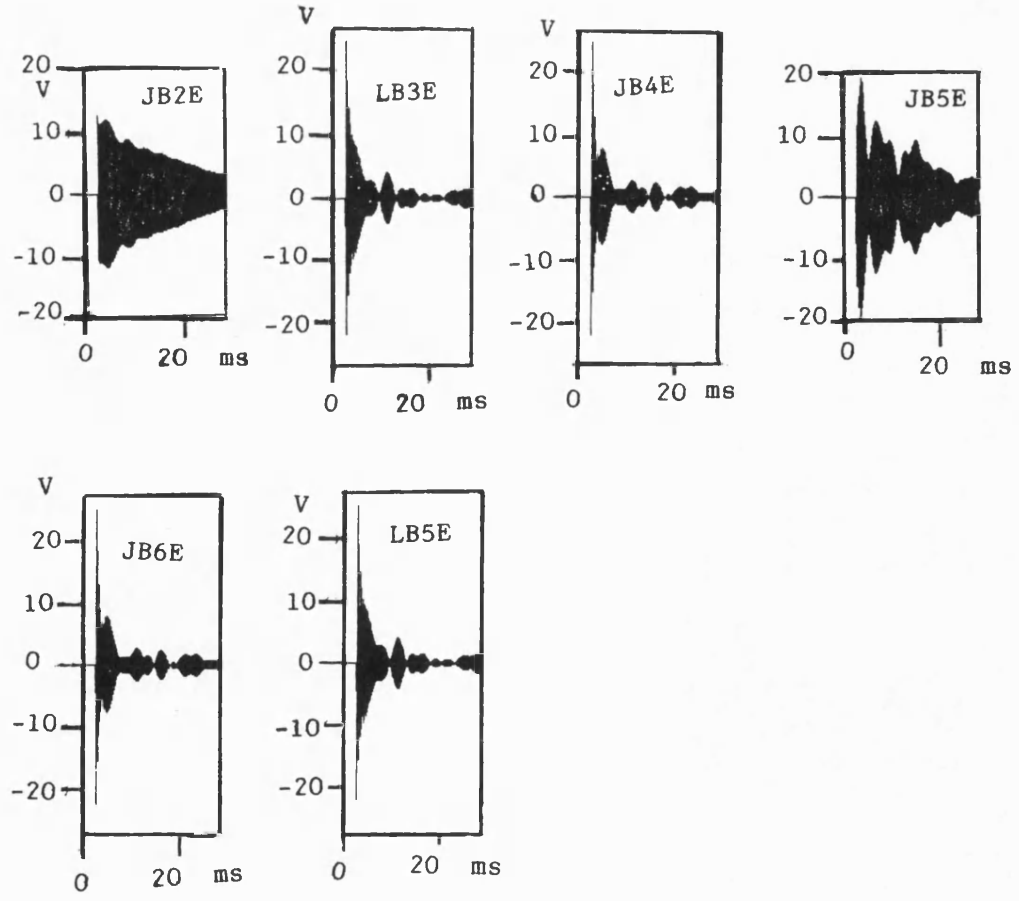


Figure 7.6 b
Comparison of output voltages from different LCR stack tuners, C_{stack}=70pF without load on terminals of the system.

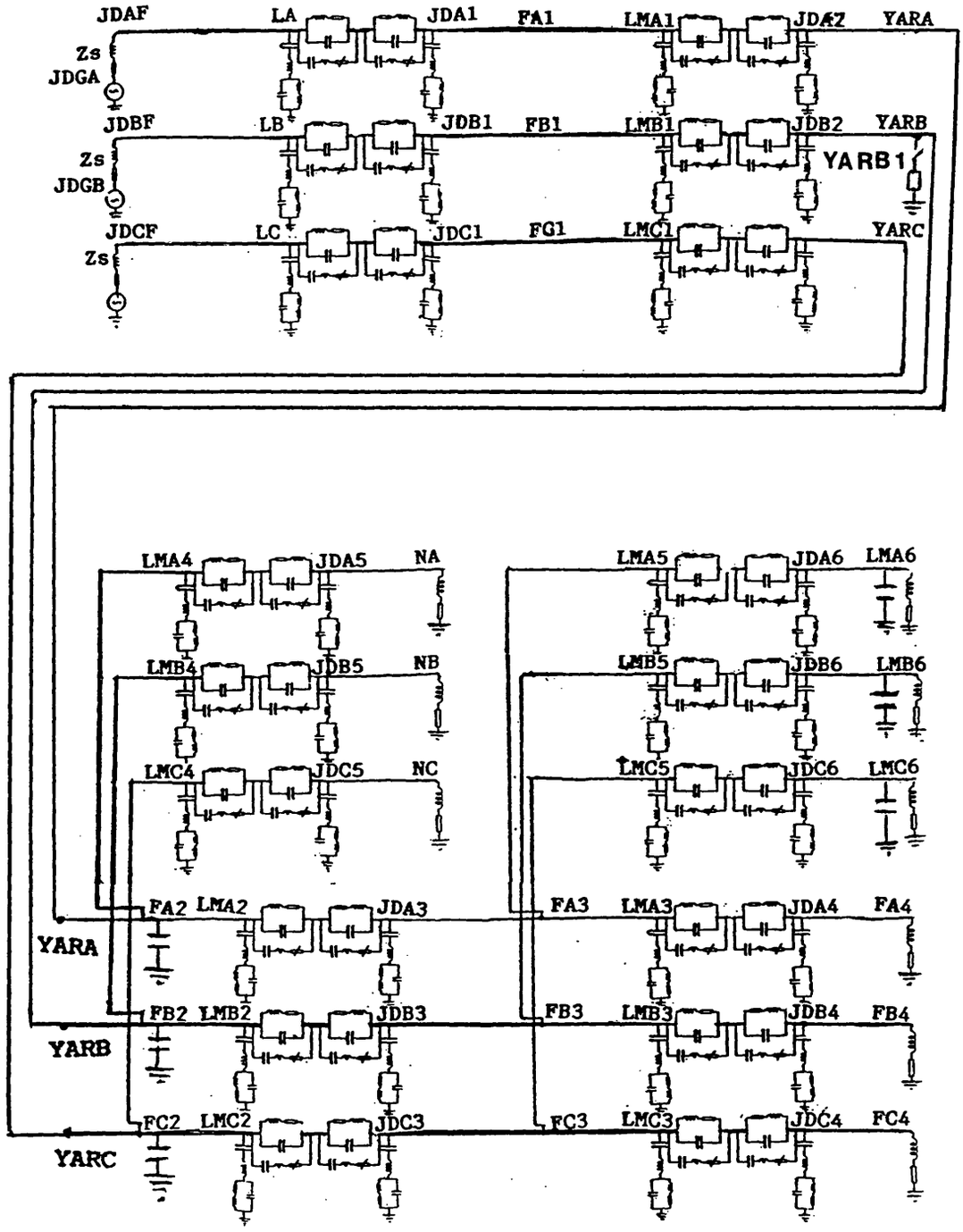


Figure 7.7
Circuit arrangement of distribution network to study effect of fault locator on steady-state performance.

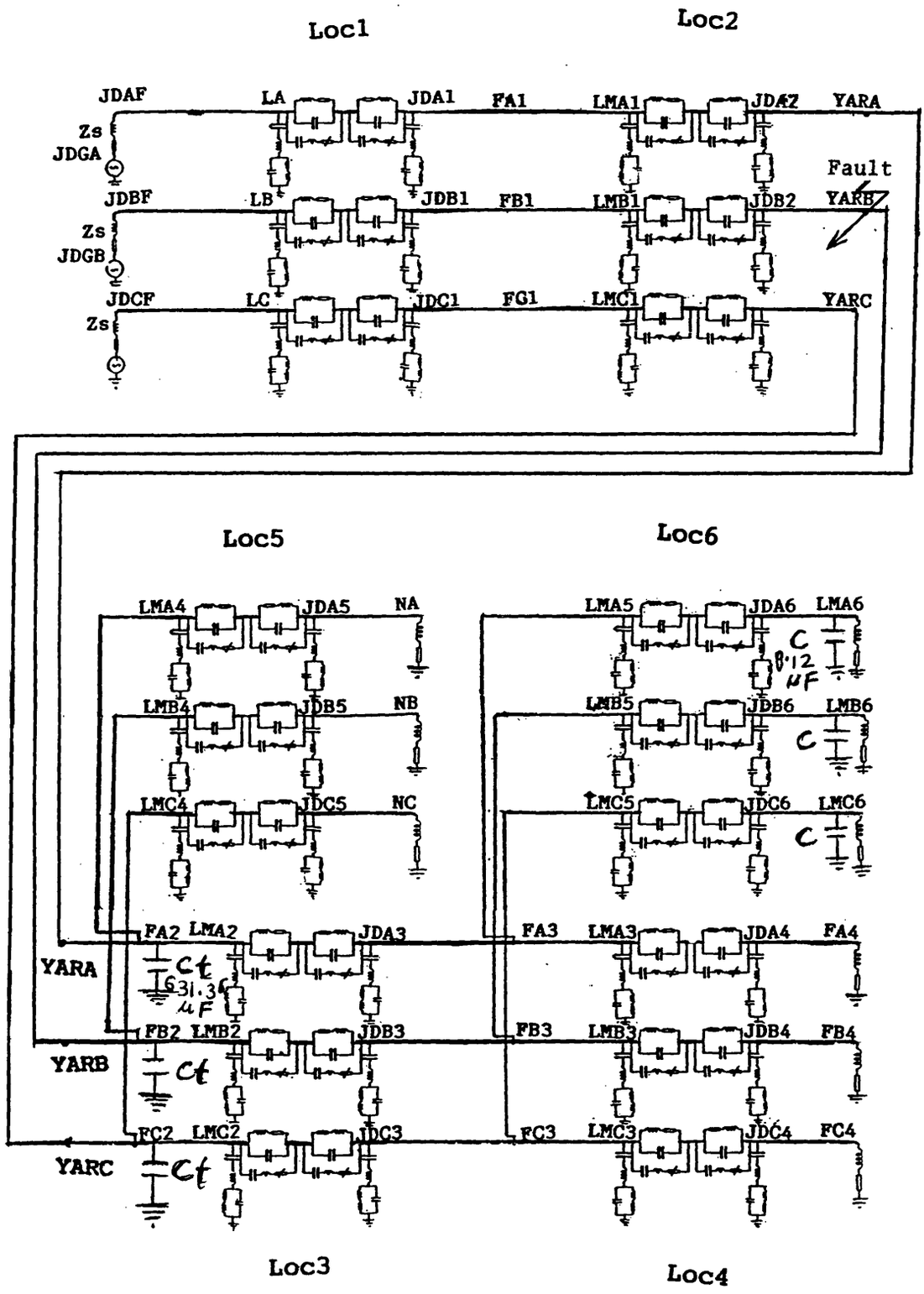


Figure 8.1
Circuit arrangement to study effect of
a capacitor bank on performance of
fault locator.

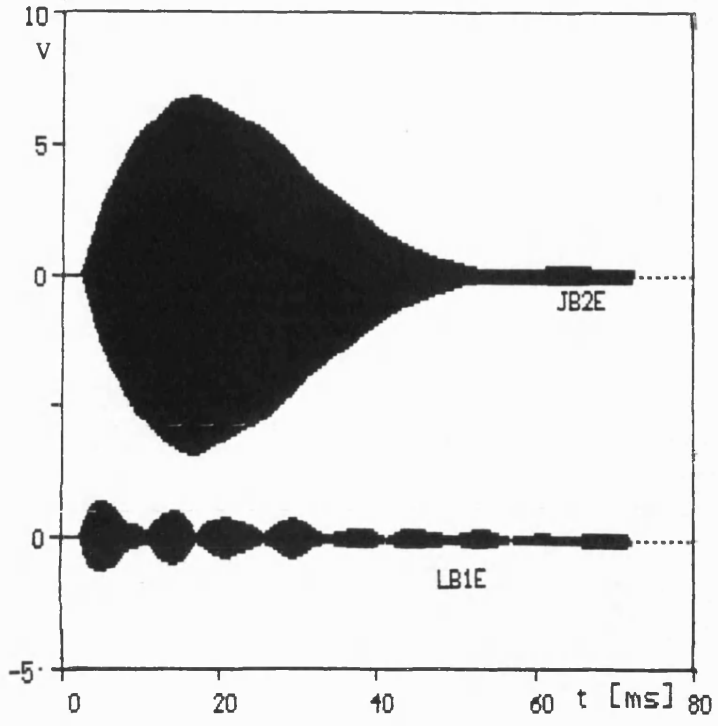


Figure 8.2a
Output signal voltage from both sides
of fault locator Loc2 close to fault.
JB2E =signal from side close to fault
LB1E =signal from side away to fault

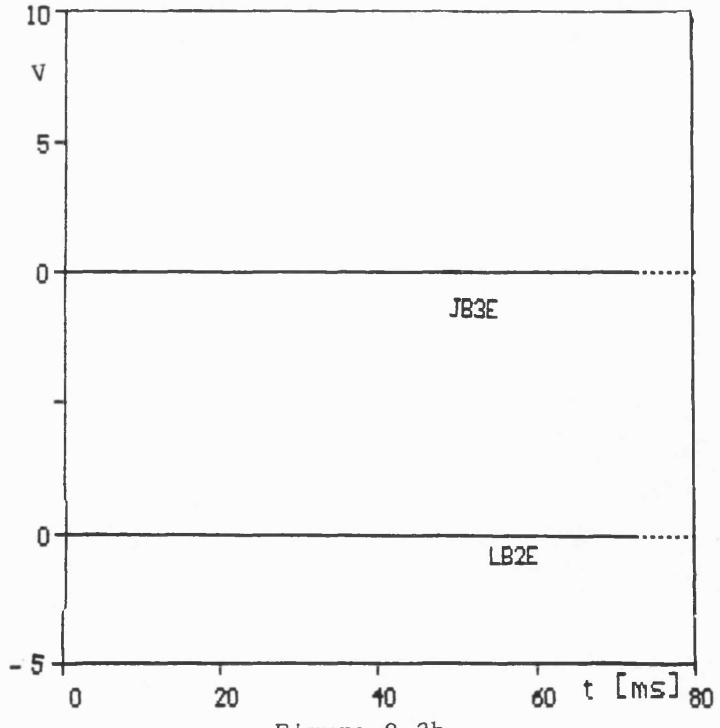


Figure 8.2b
Output signal voltage from both sides
of fault locator Loc3 close to fault.
LB2E =signal from side close to fault
JB3E =signal from side away to fault

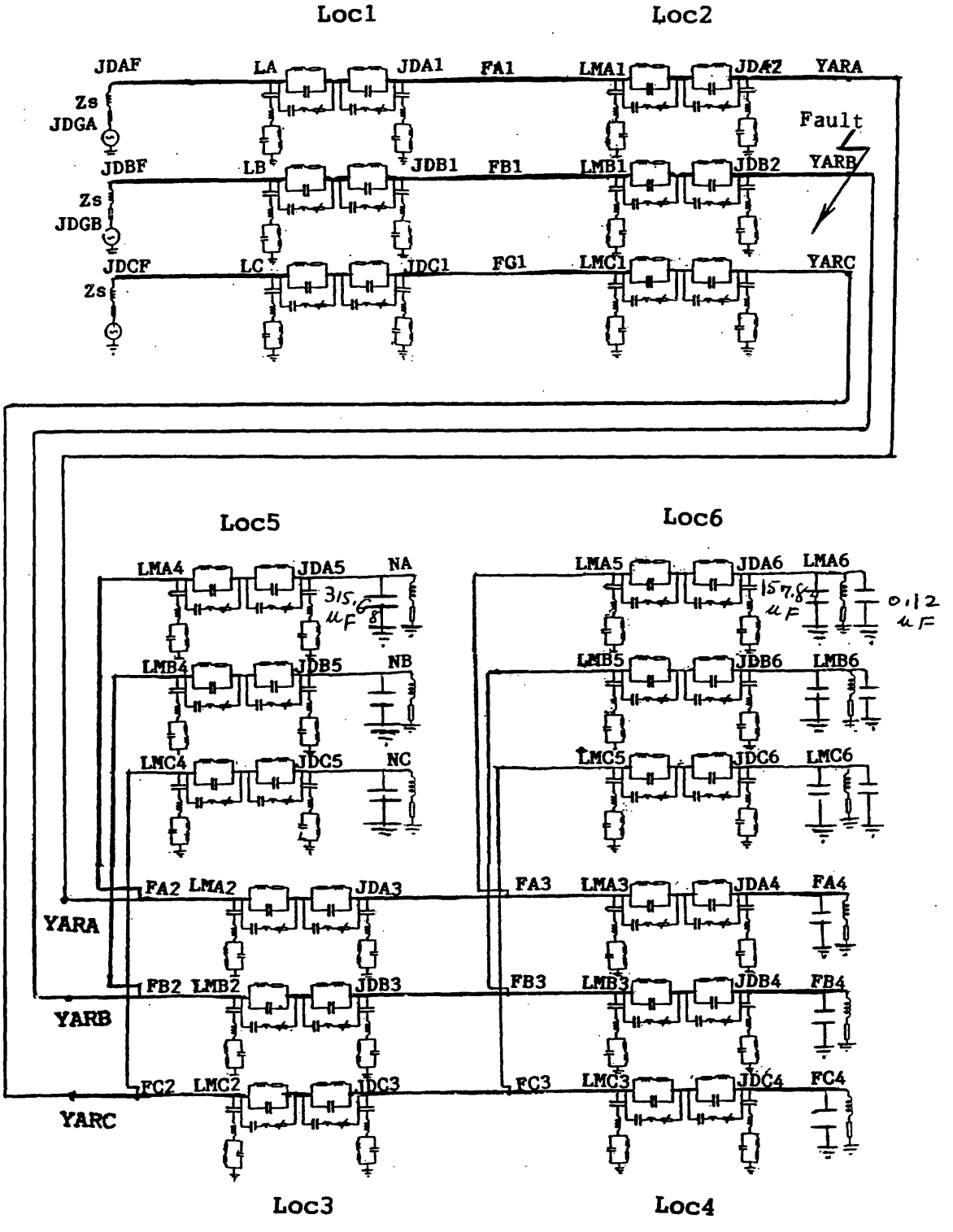


Figure 8.3
Circuit arrangement to study effect of
a capacitor bank on performance of
fault locator.

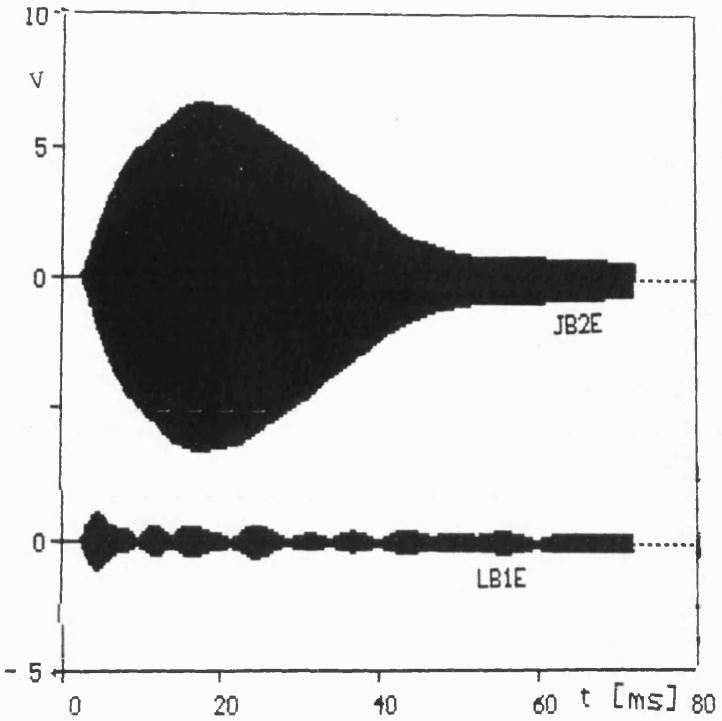


Figure 8.4a
Output signal voltage from both sides
of fault locator Loc2 close to fault.
JB2E =signal from side close to fault
LB1E =signal from side away to fault

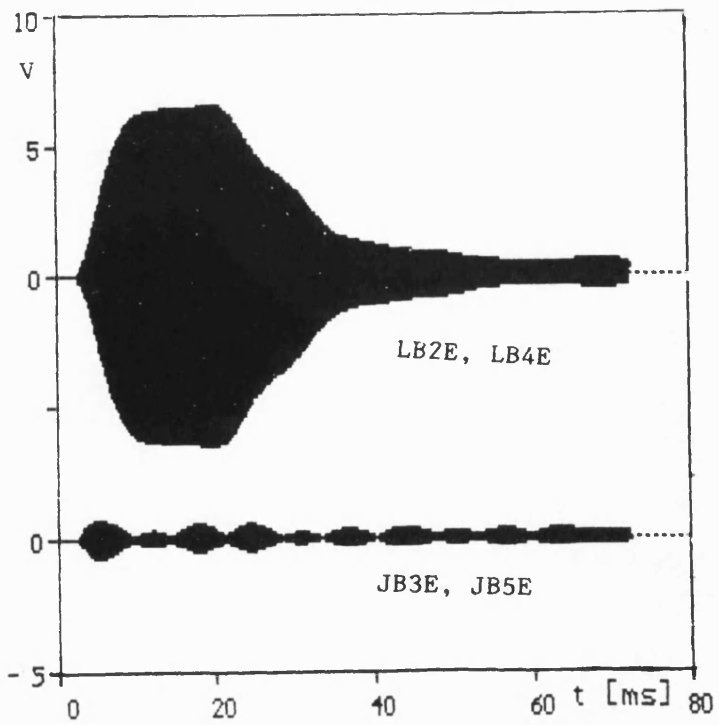


Figure 8.4b
Output signal voltage from both sides of
fault locators Loc3 & Loc5 close to fault.
LB2E, LB4E =signal from side close to fault
JB3E, JB5E =signal from side away from fault

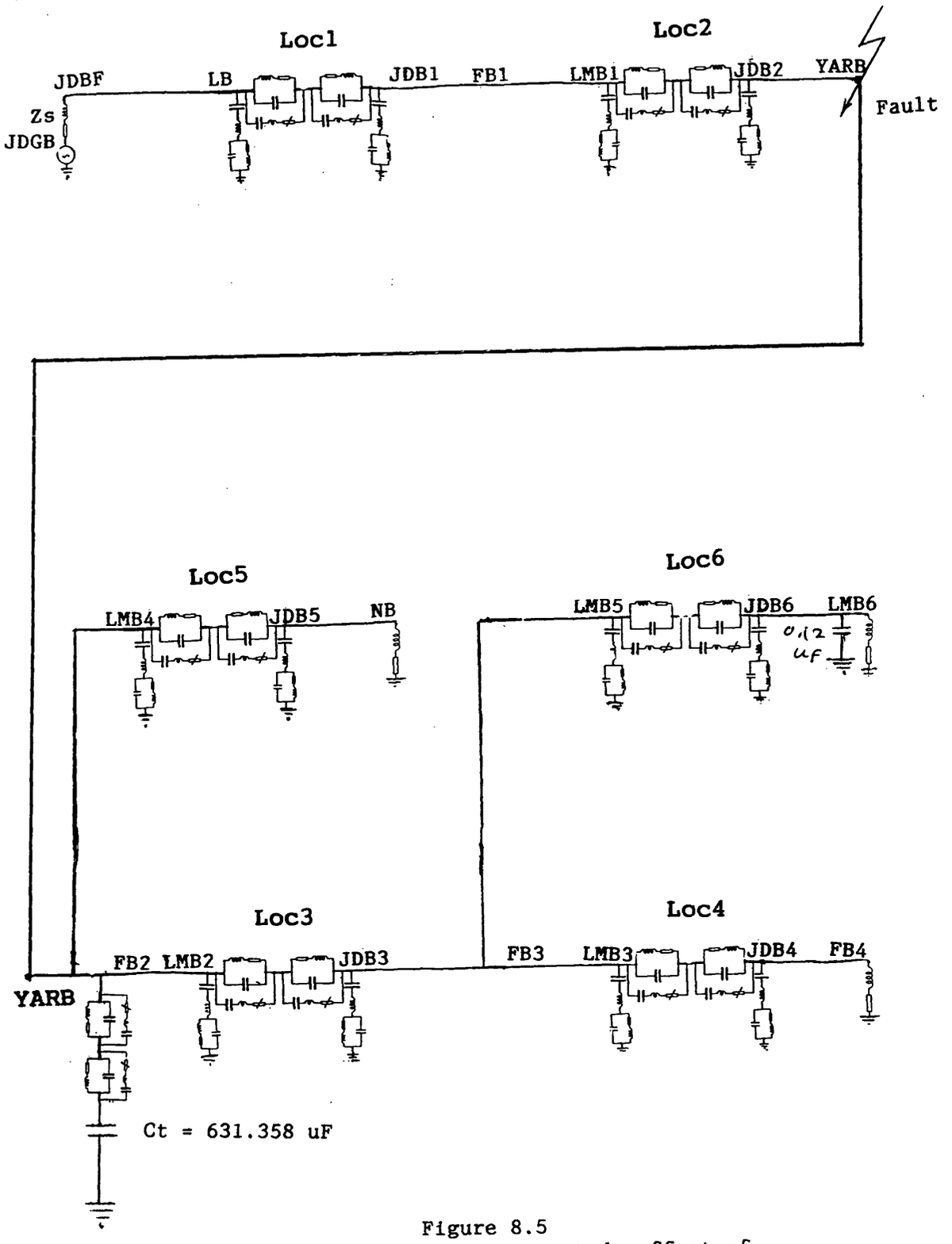


Figure 8.5
Circuit arrangement to study effect of
a capacitor bank on performance of
fault locator.

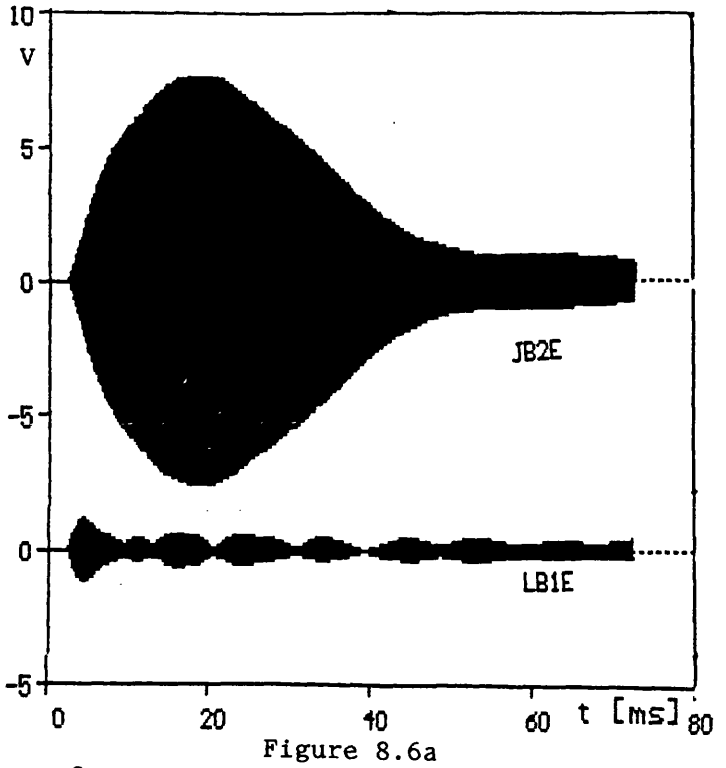


Figure 8.6a
Output signal voltage from both sides of fault locator Loc2 close to fault.
JB2E =signal from side close to fault
LB1E =signal from side away to fault

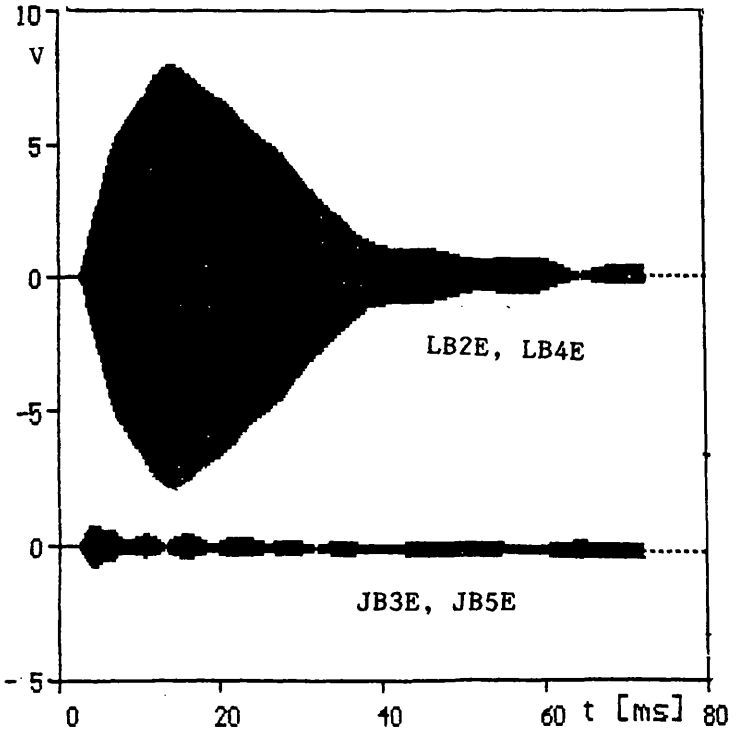


Figure 8.6b
Output signal voltage from both sides of fault locator Loc3 & Loc5 close to fault.
LB2E, LB4E =signal from side close to fault
JB3E, JB5E =signal from side away from fault

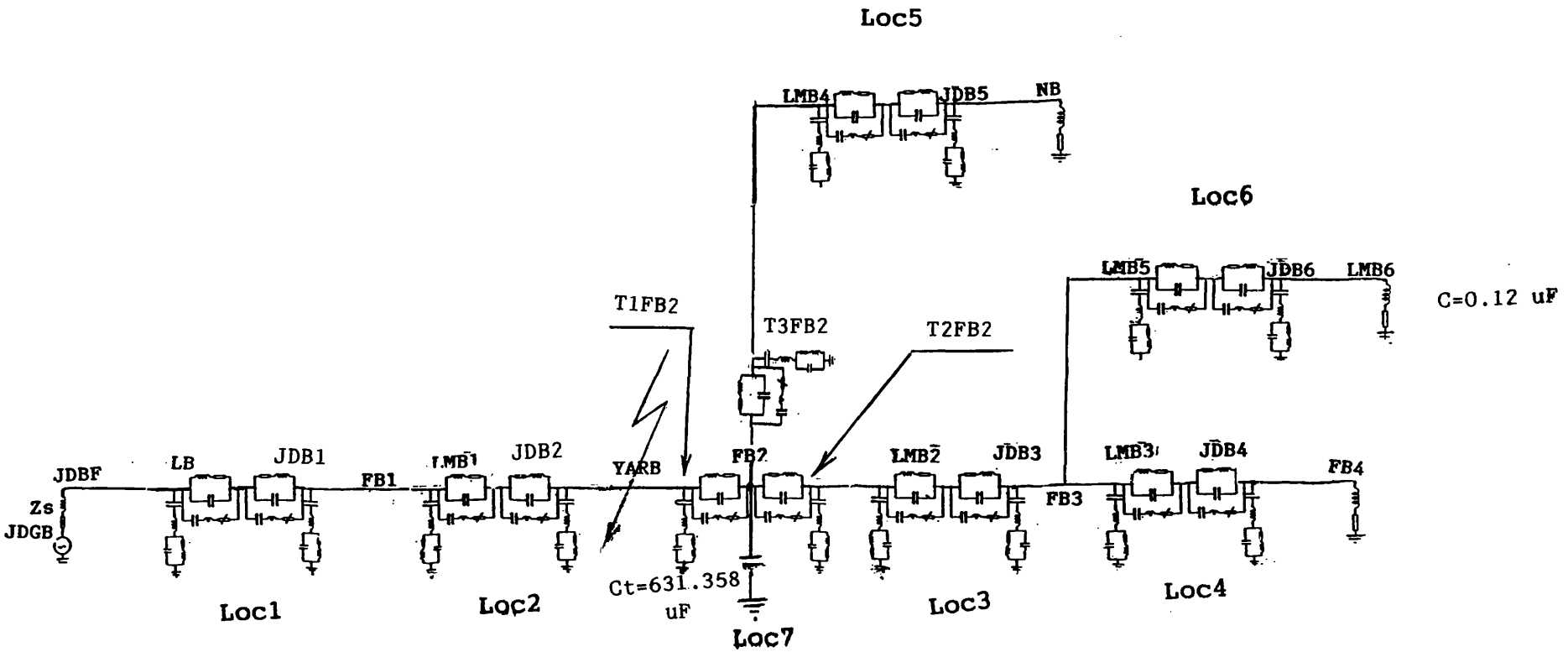


Figure 8.7
Circuit arrangement (phase B only) to study effect of a capacitor bank on performance of fault locator.

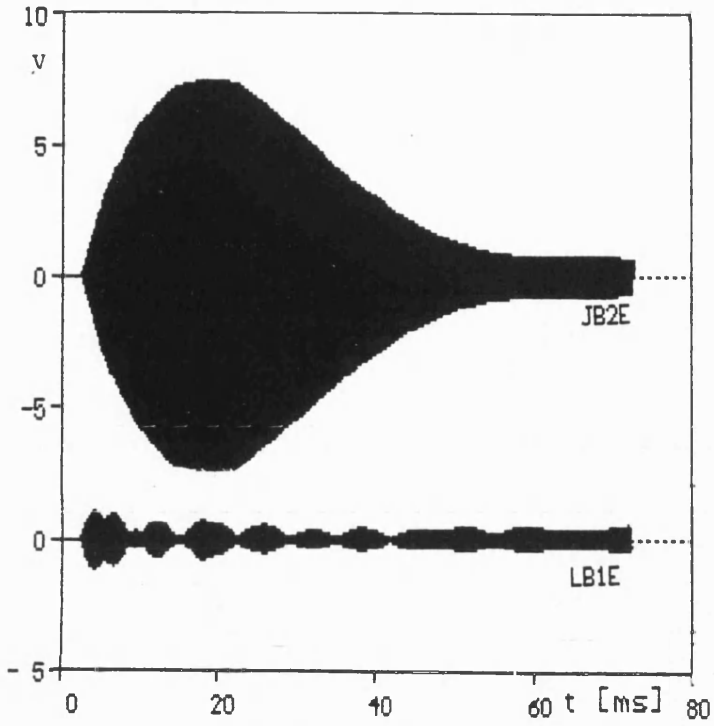


Figure 8.8a
Output signal voltage from both sides
of fault locator Loc2 close to fault.
JB2E =signal from side close to fault
LB1E =signal from side away to fault

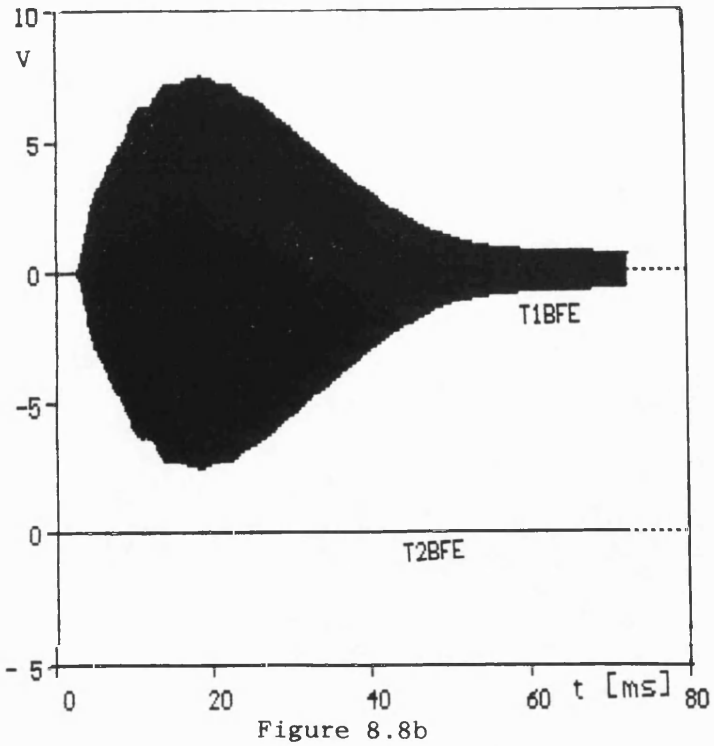


Figure 8.8b
Output signal voltage from both sides
of fault locator Loc7 close to fault.
T1BFE=signal from side close to fault
T2BFE=signal from side away to fault

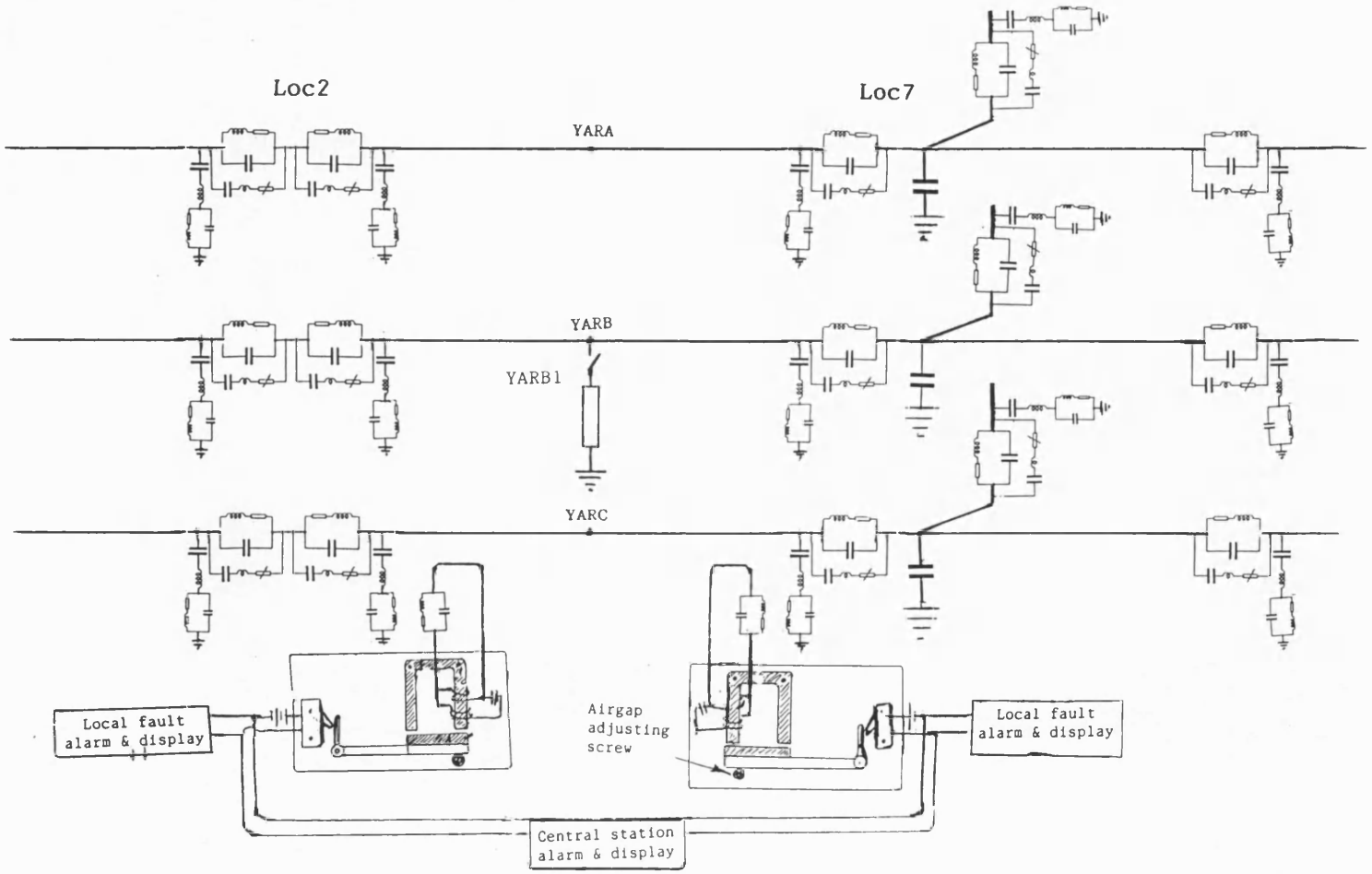


Figure 9.1 a
Circuit arrangement for single phase type application of the fault locator

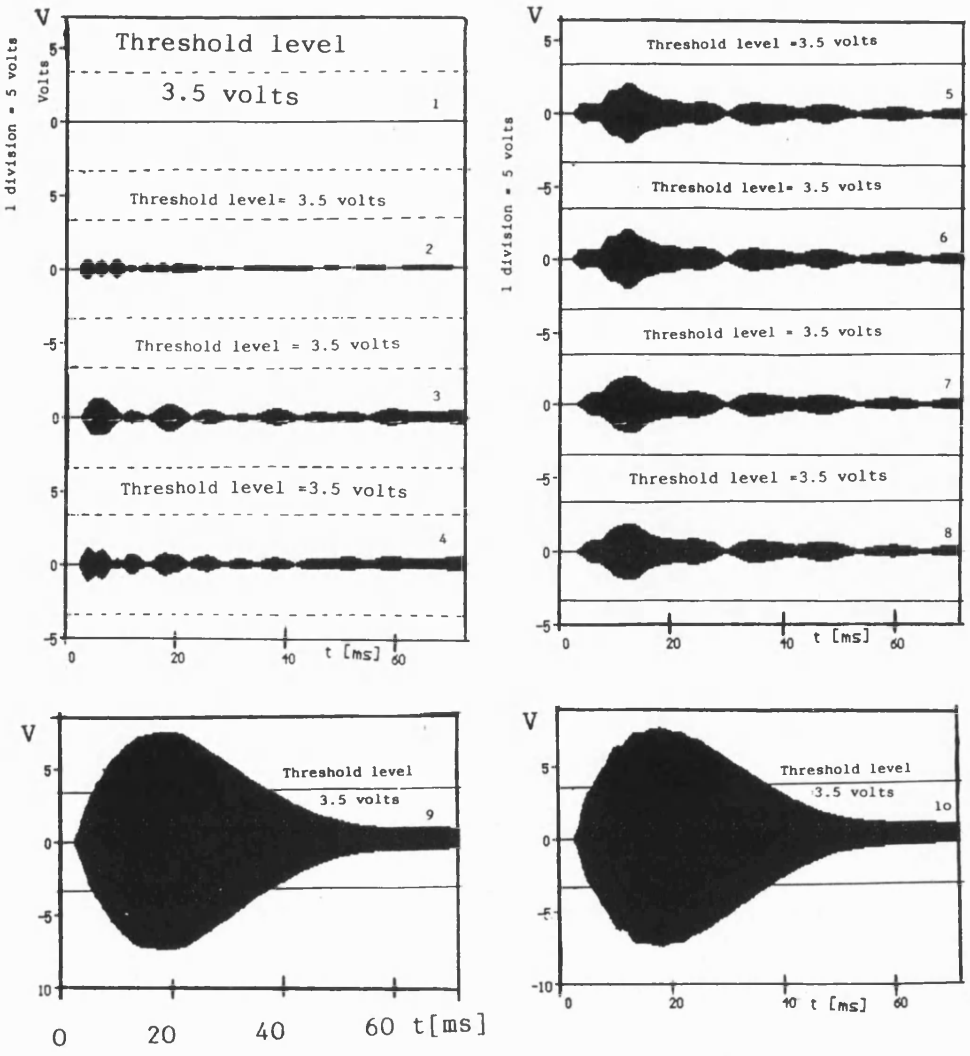


Figure 9.1 b
Fault locator output signals from stack tuners

1 Out put signals from nodes AFE, CFE, JA1E, JC1E, LA1E, LC1E, JA2E,JB2E,JC2E,LA2E,LB2E,LC2E, JA3E,JB3E,JC3E,LA3E,LB3E,LC3E, JA4E,JB4E,JC4E,LA4E,LB4E,LC4E, JA5E,JB5E,JC5E,LA5E,LB5E,LC5E, JA6E,JB6E,JC6E,T2AFE,T2BFE,T2CFE, T3AFE,T3BFE,T3CFE

2 Output signal BFE
3 Output signal JB1E
4 Output signal LB1E
5 Output signal JA2E
6 Output signal JC2E
7 Output signal T1AFE
8 Output signal T1CFE
9 Output signal JB2E
10 Output signal T1BFE

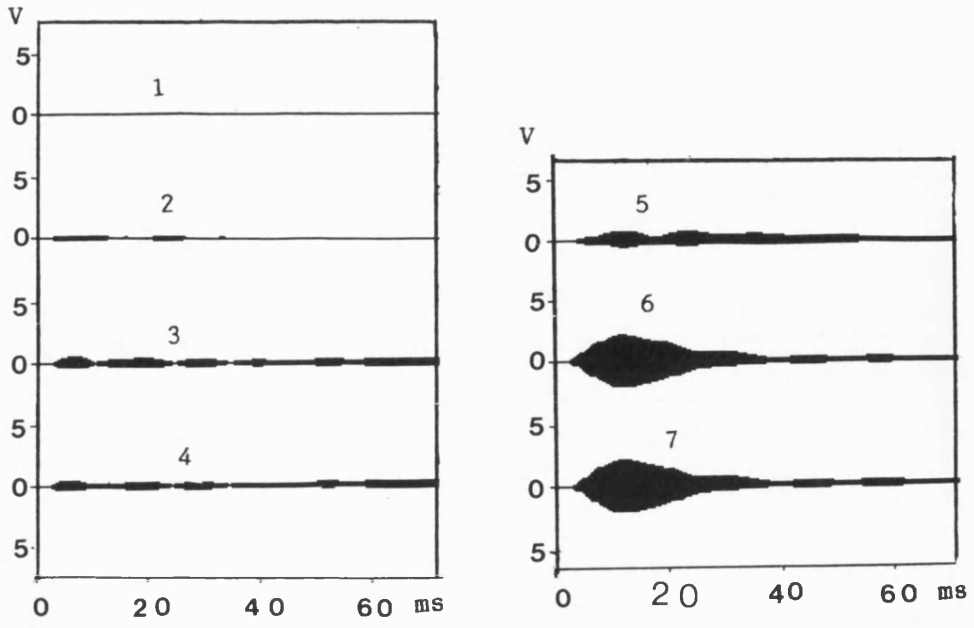


Figure 9.1 c
Per phase fault locator outputs for line to ground fault through 1000 ohms resistance.

1. Output voltage signals near zero (0.0)
   LB2E, JB3E, LB3E, JB4E, LB4E, JB5E,
   LB5E, JB6E, T2BFE, T3BFE

2. Output voltage signal BFE

3. Output voltage signal JB1E

4. Output voltage signal LB1E

5. Output voltage signals T1CFE, T1AFE, JA2E, JC2E

6. Output voltage signal JB2E

7. Output voltage signal T1BFE

..... Threshold level of voltage = 1.0 volt not shown

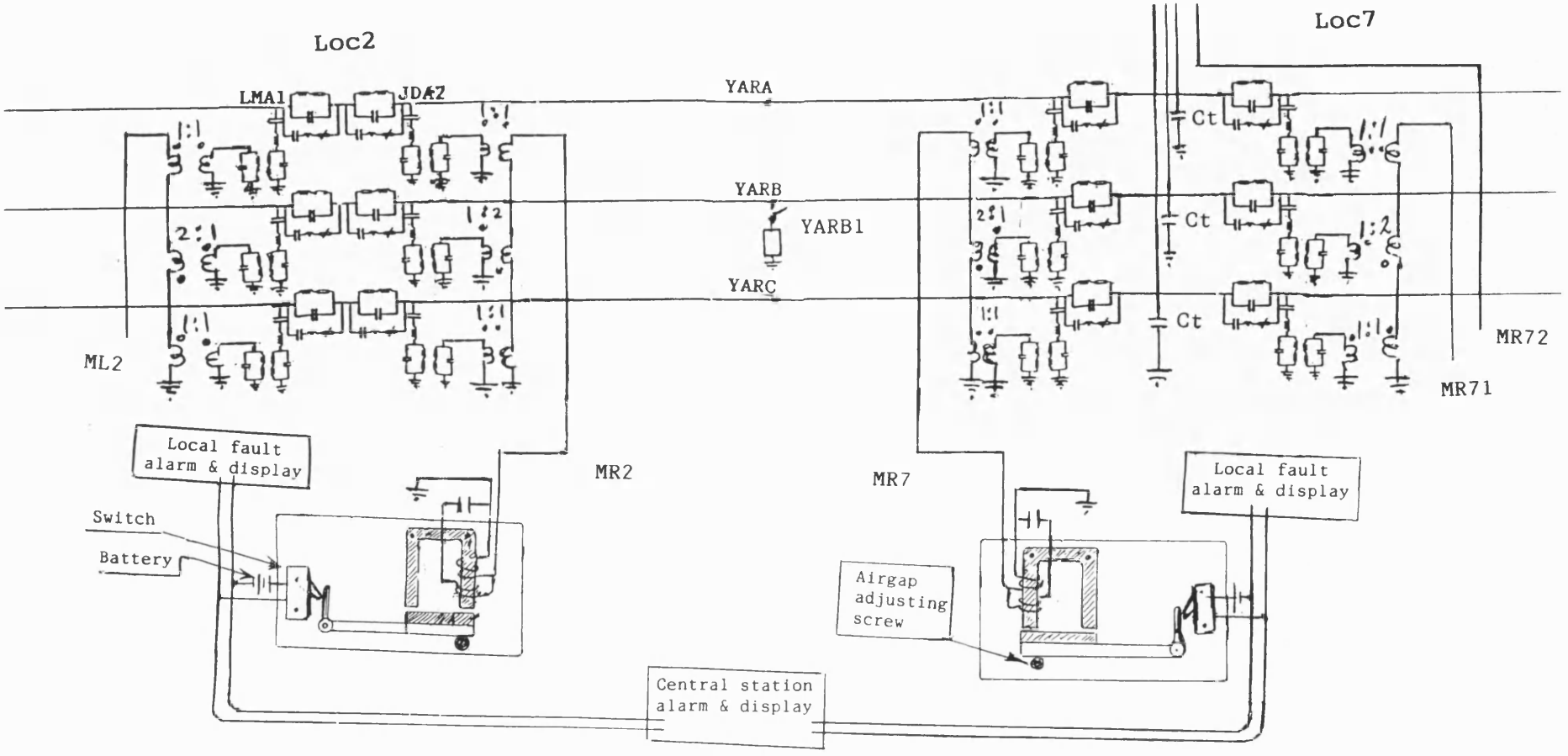


Figure 9.2 a
Circuit arrangement for the modal type application of the fault locator

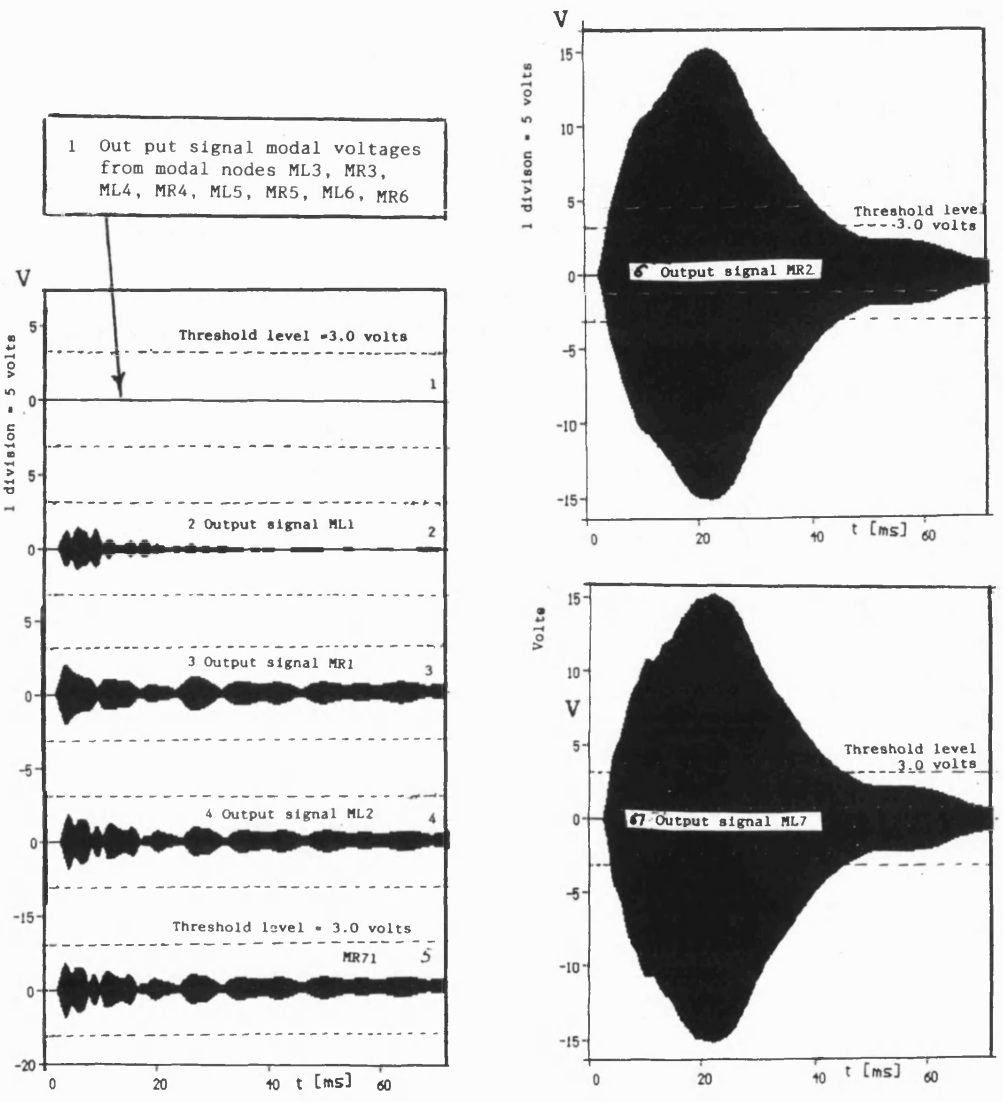


Figure 9.2 b

Fault locator output signals from stack tuners

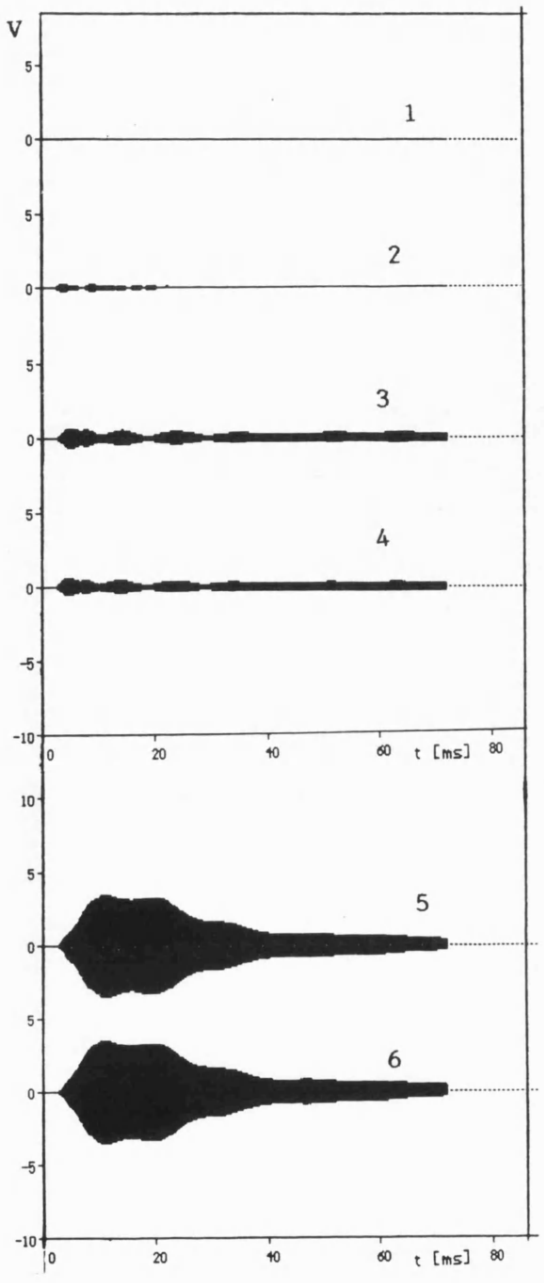


Figure 9.2 c
Modal fault locator output voltages for line to ground fault through 1000 ohms resistance.

1. Output voltage signals near zero (0.0)
   ML3, MR3, ML4, MR4, ML5, MR5, ML6,
   MR6, MR71, MR72

2. Output signal voltage ML1

3. Output voltage signal MR1

4. Output voltage signal ML2

5. Output voltage signal MR2

6. Output voltage signal ML7

..... Threshold level of voltage = 1.0 volt not shown

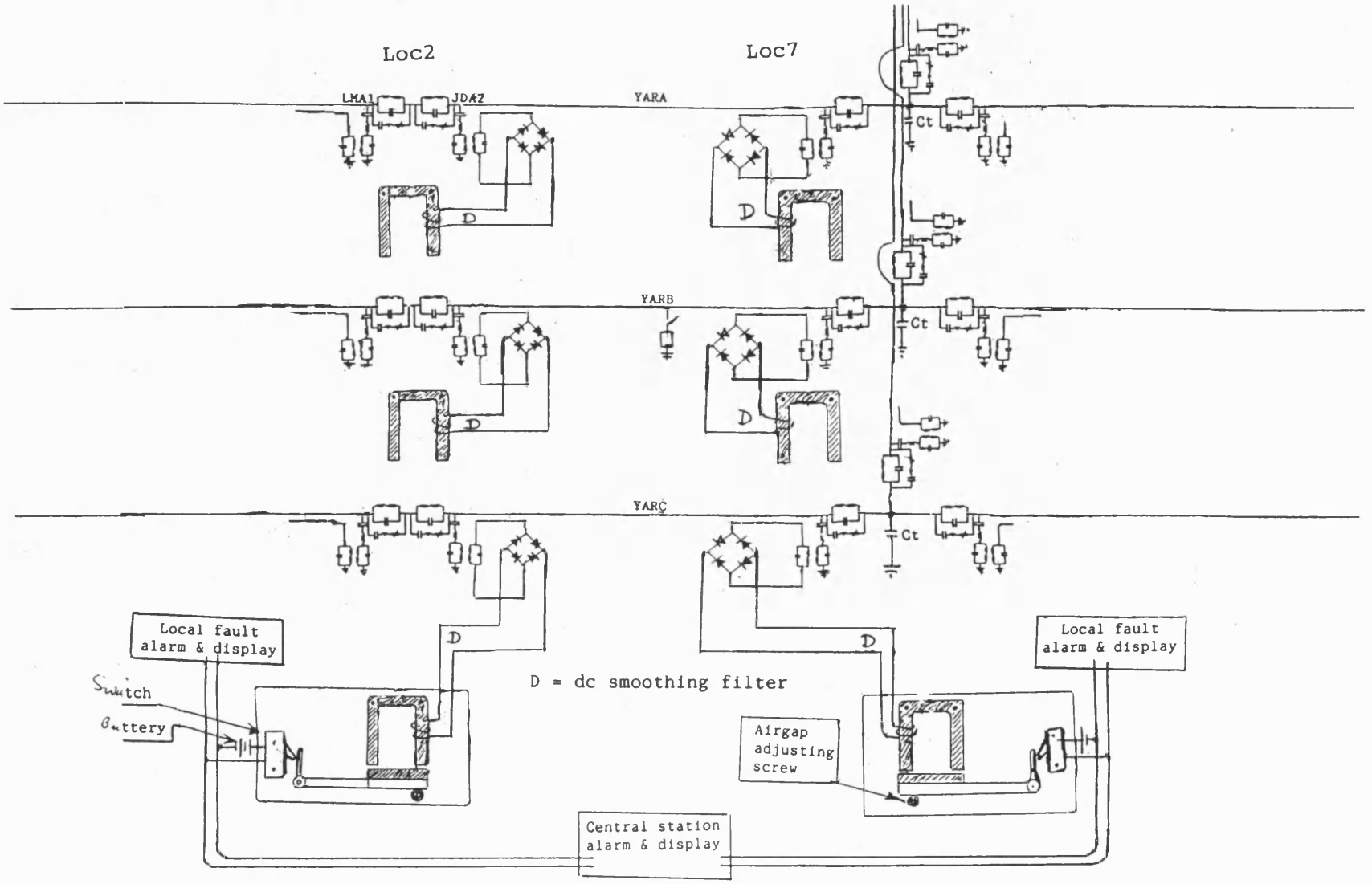


Figure 9.3 a
Circuit arrangement for 1-phase rectified type application of the fault locator

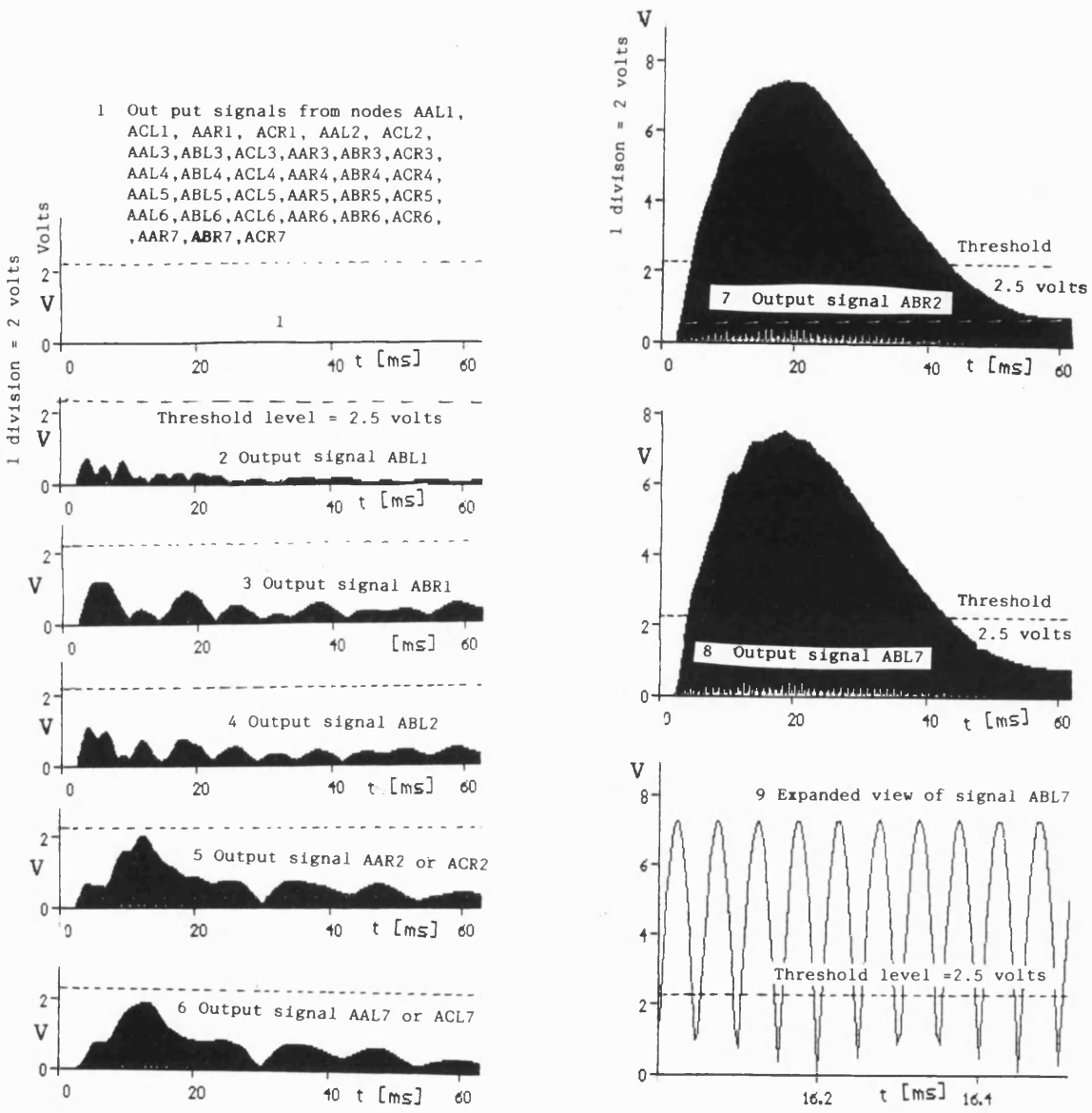


Figure 9.3 b

Fault locator output signals from stack tuners

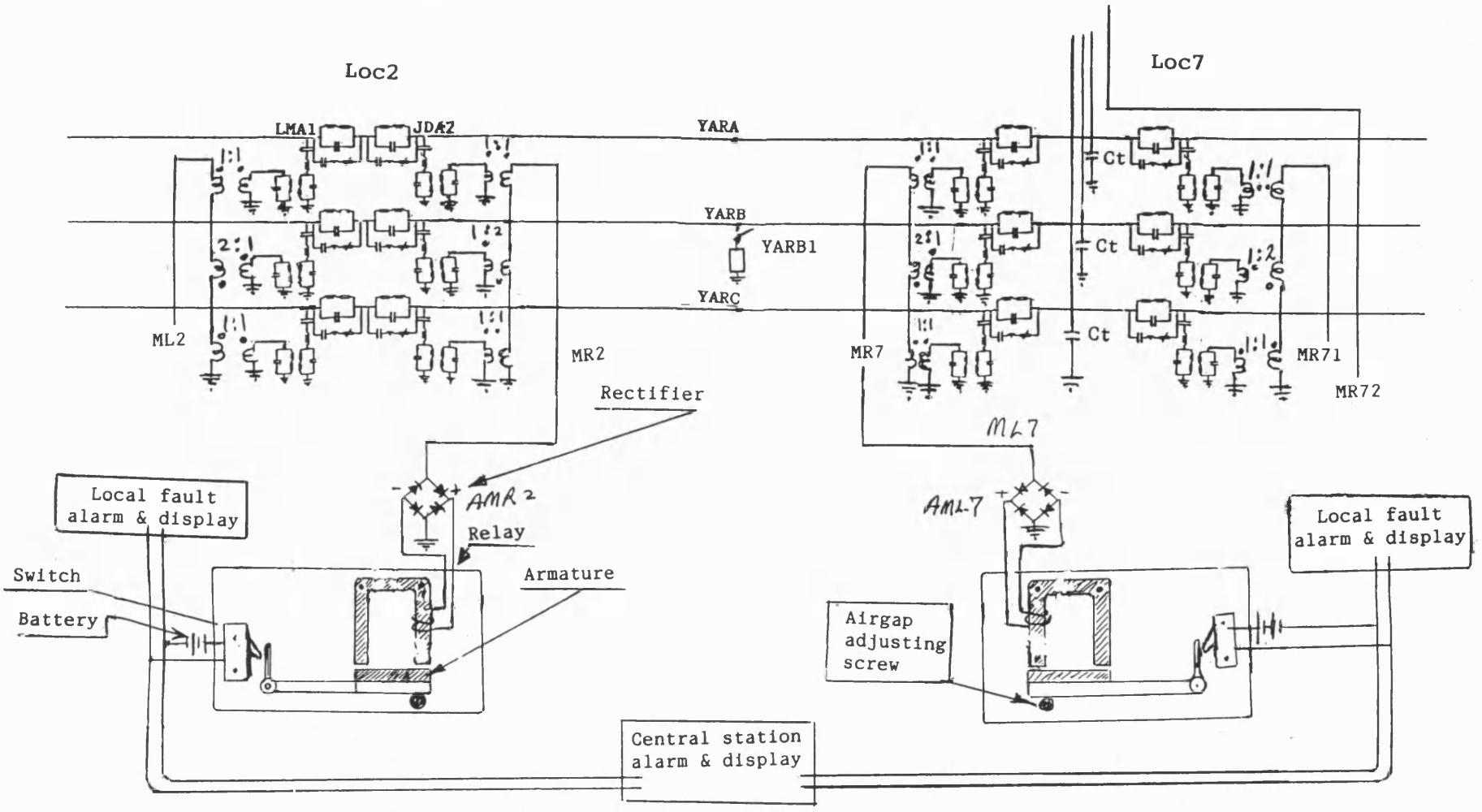


Figure 9.4 a
Circuit arrangement for modal type application of the fault locator

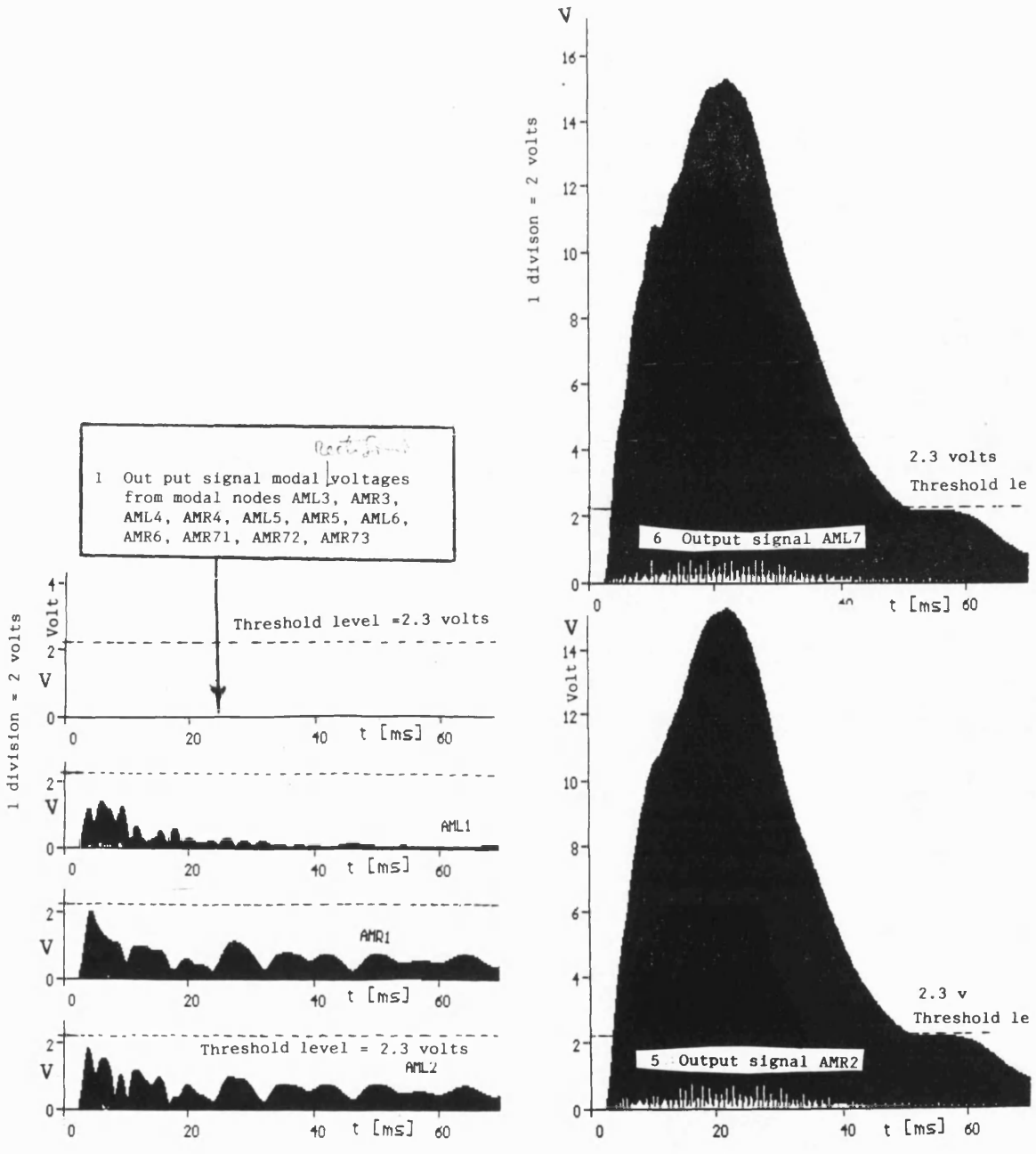


Figure 9.4 b

Fault locator output signals from modal stack tuners after rectification

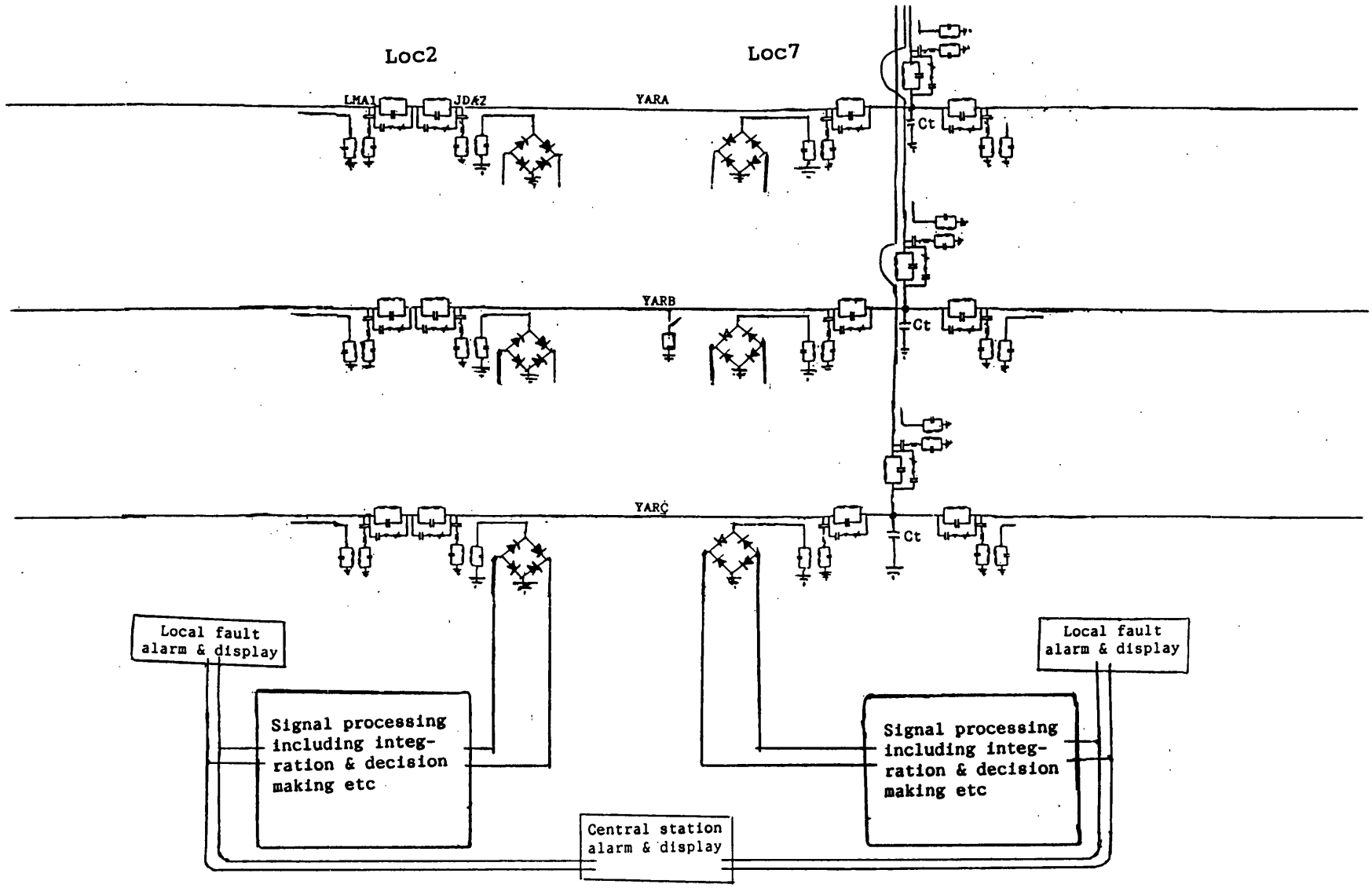


Figure 9.5 a
Circuit arrangement for 1-phase integration type application of the fault locator

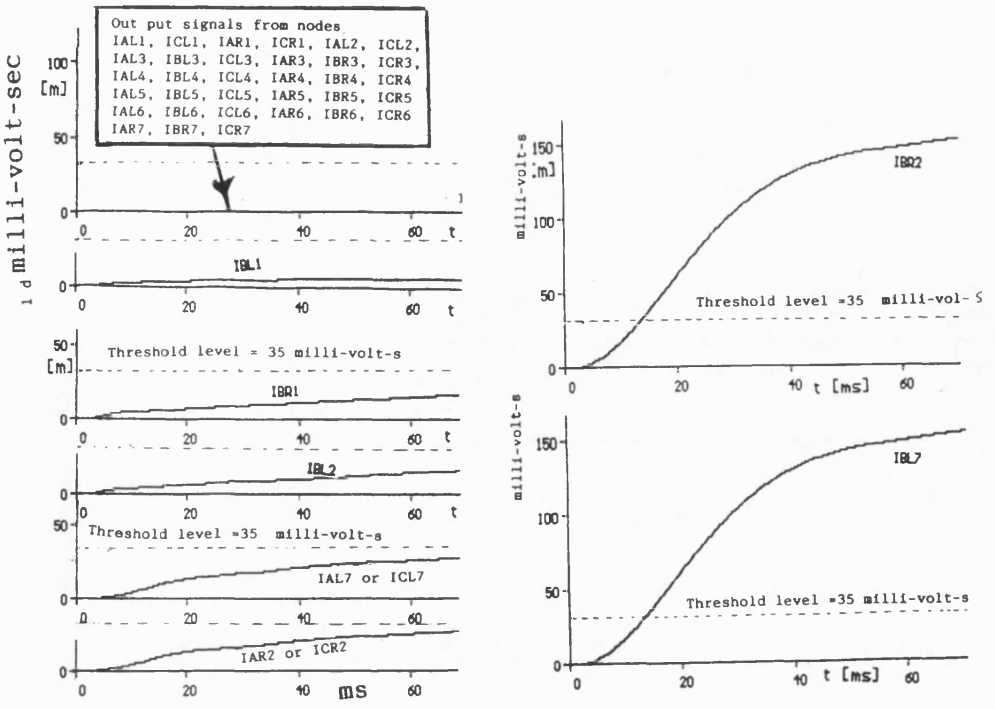
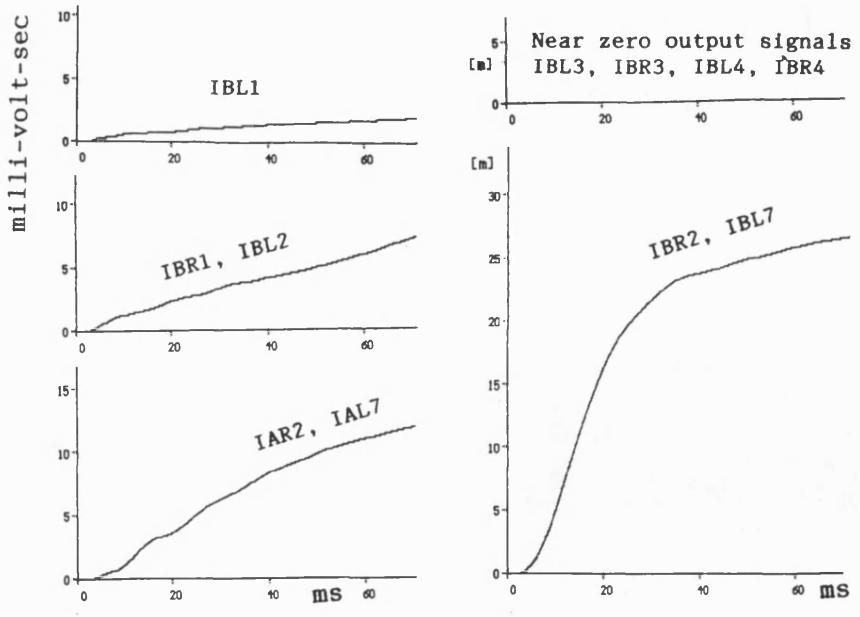
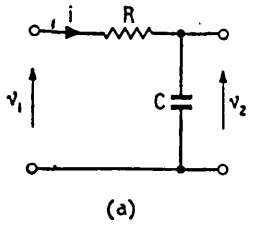


Figure 9.5 b
Fault locator signal outputs for single phase integration type application of the fault locator

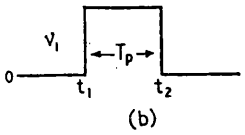


Threshold level is 10 m-V-s

Figure 9.5 c
Fault locator per phase output signals in line to ground fault through 1000 ohms fault resistance



(a)



(b)

$$v_1 = iR + \frac{1}{C}\int i\,.\,dt$$

$$v_2 = \frac{1}{C}\int i\,.\,dt$$

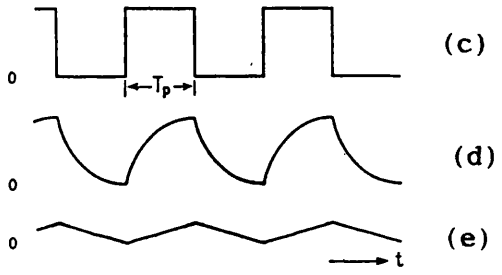


Figure 9.5d
The effect on a square wave of the integrator circuit
(a) The integrator circuit
(b) Input waveform of single square wave impulse
(c) Input waveform train
(d) Output waveform when $T_p = 5CR$;
(e) Output waveform when $T_p = \frac{1}{10}CR$

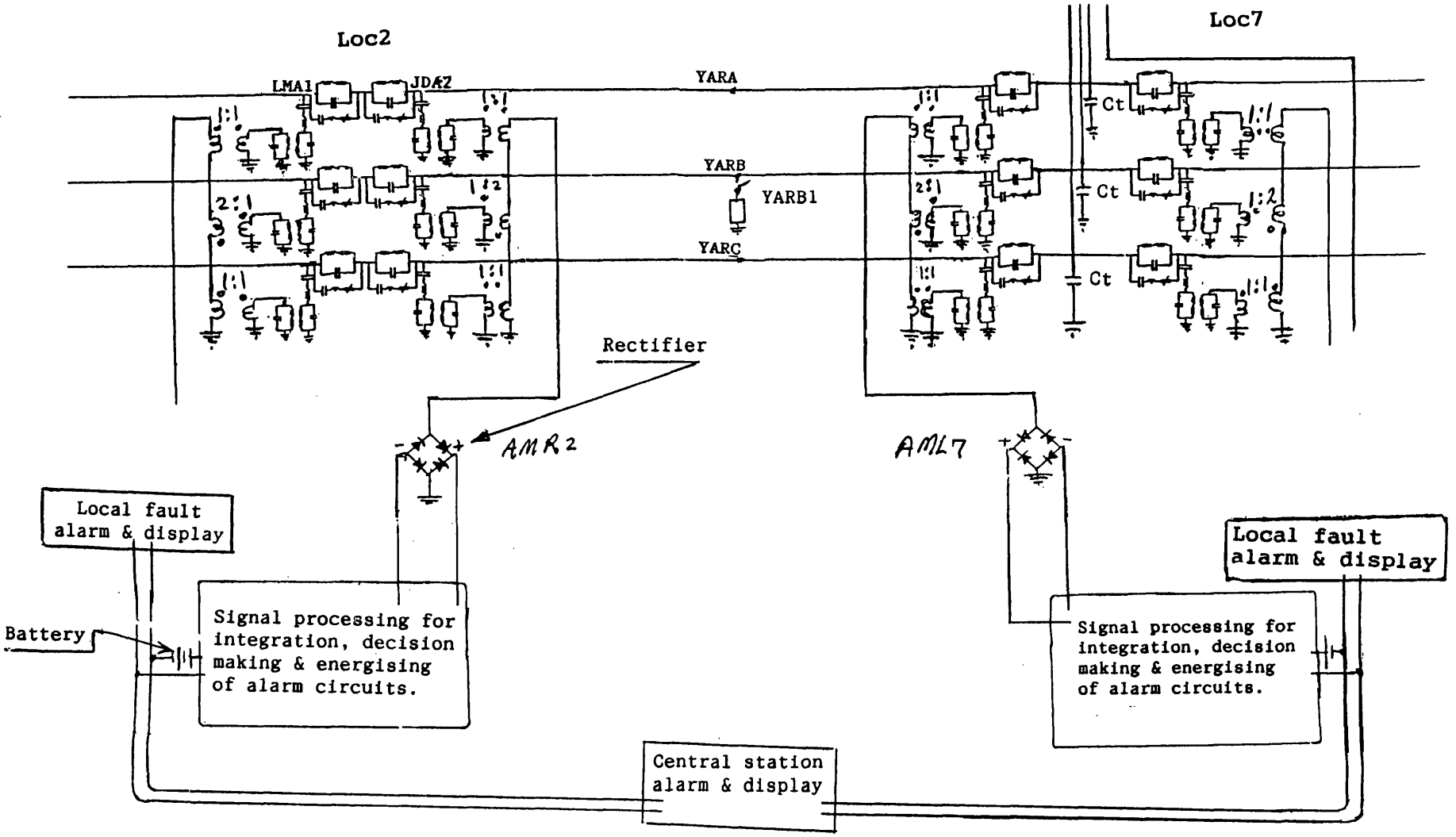


Figure 9.6a

Circuit arrangement to study modal integration type application of fault locator

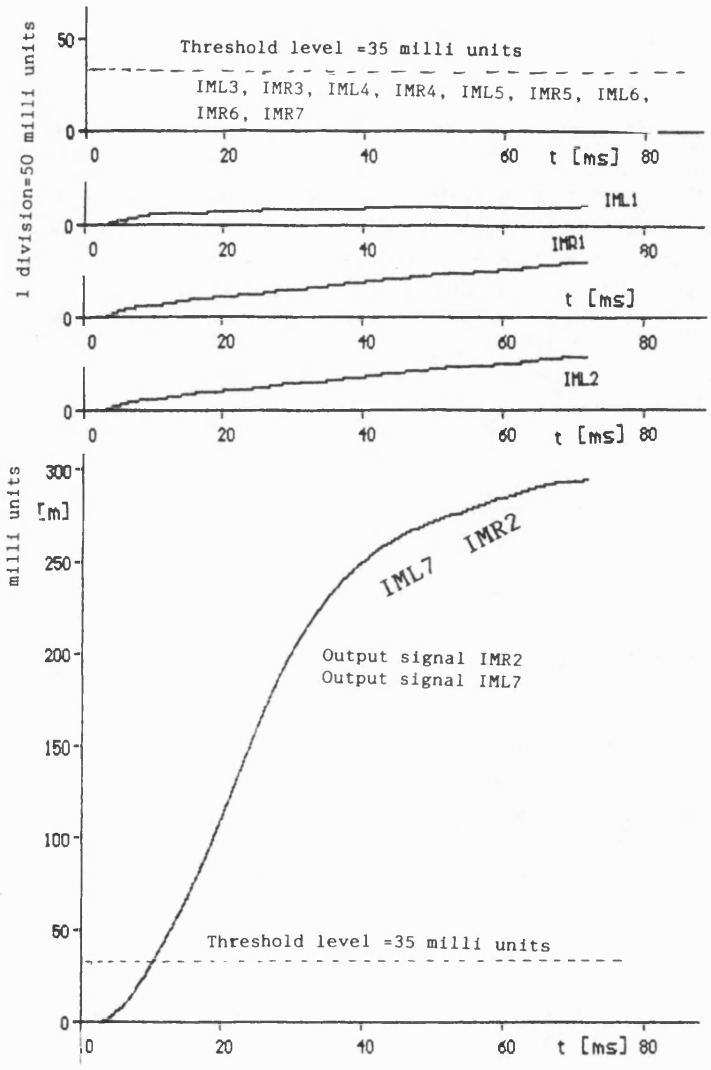


Figure 9.6 b

Various signal processed output signals which are obtained by integrating modal rectified voltages.

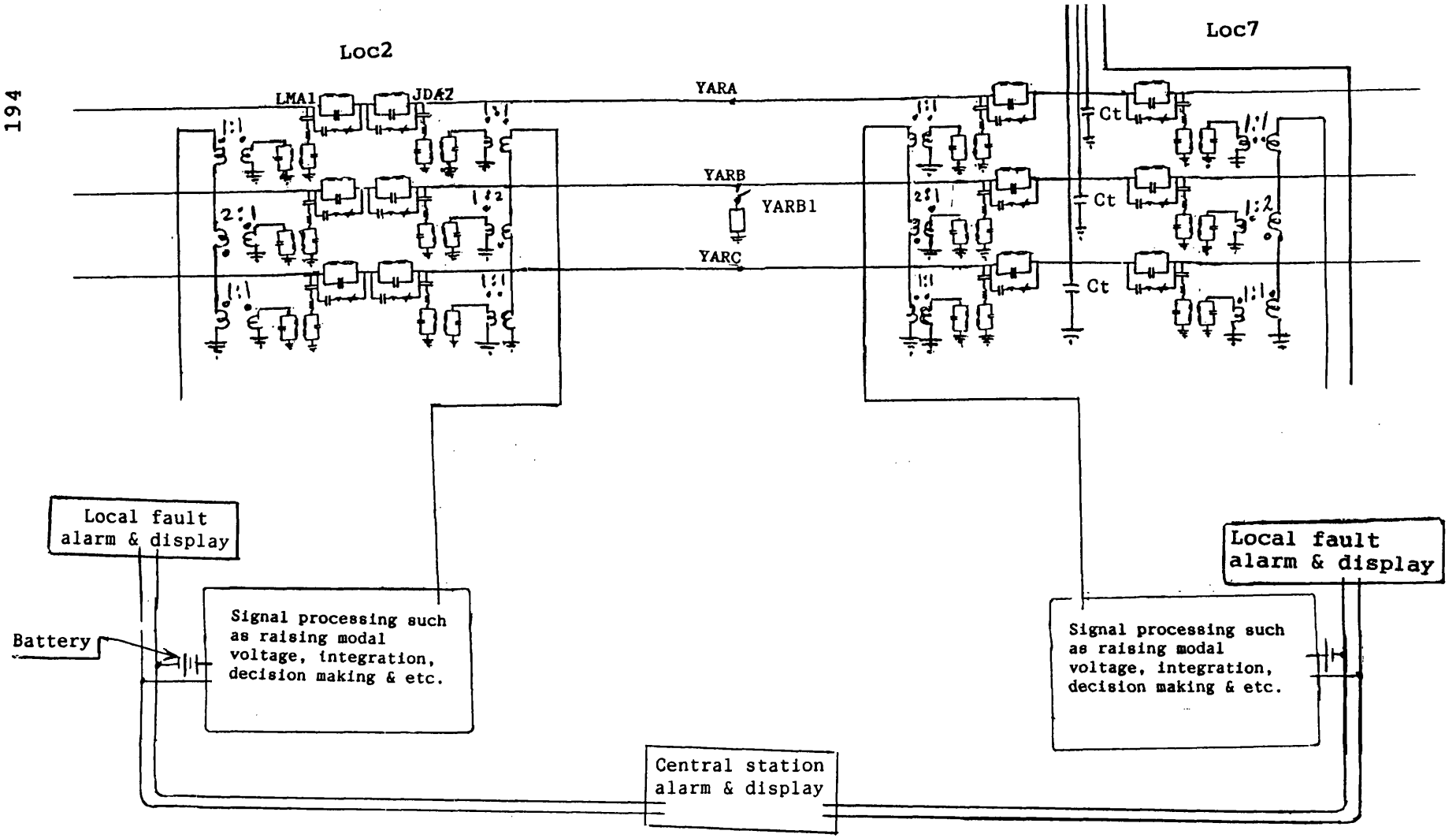


Figure 9.7a
Modal raised to power r integrated type application

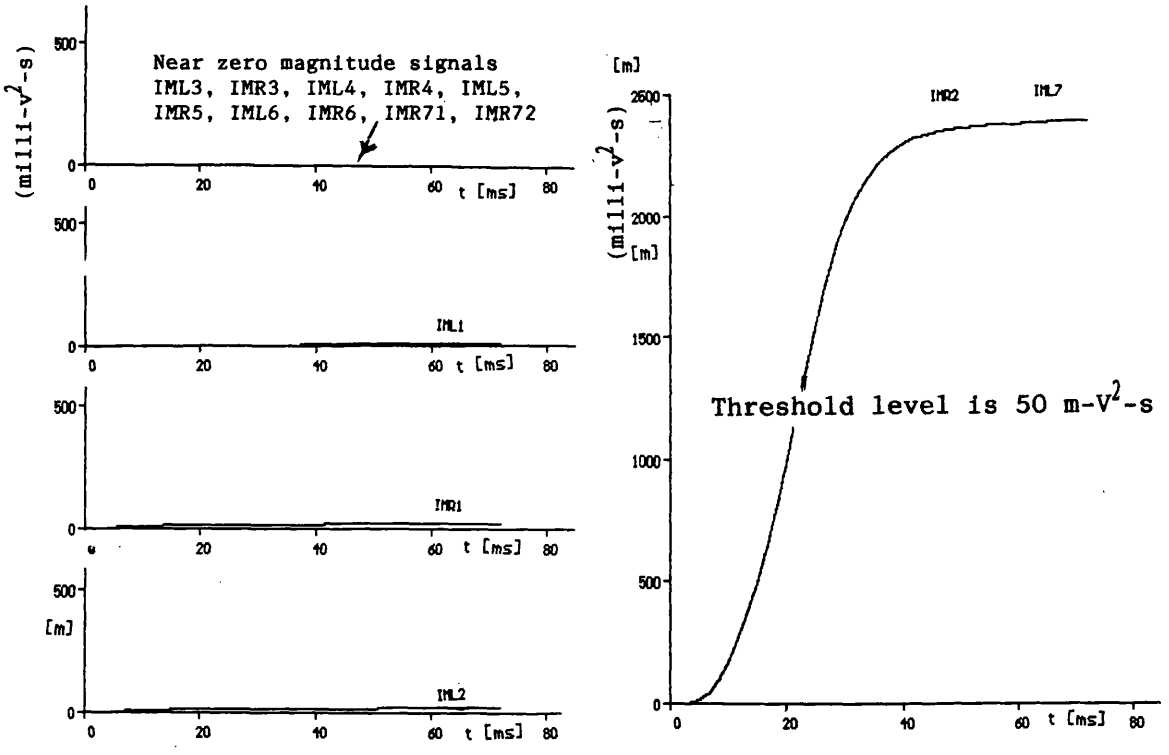


Figure 9.7b

Modal energy (r=2) integrated line to earth fault

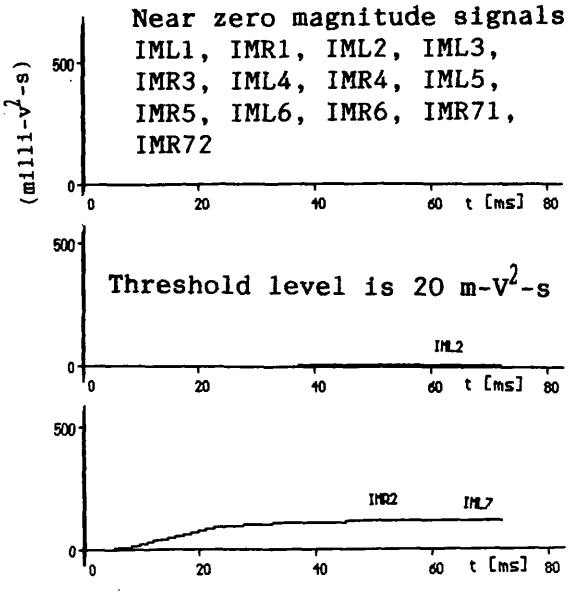


Figure 9.7 c

Modal energy (r=2) integrated line to earth fault with fault resistnce of 1000 ohms

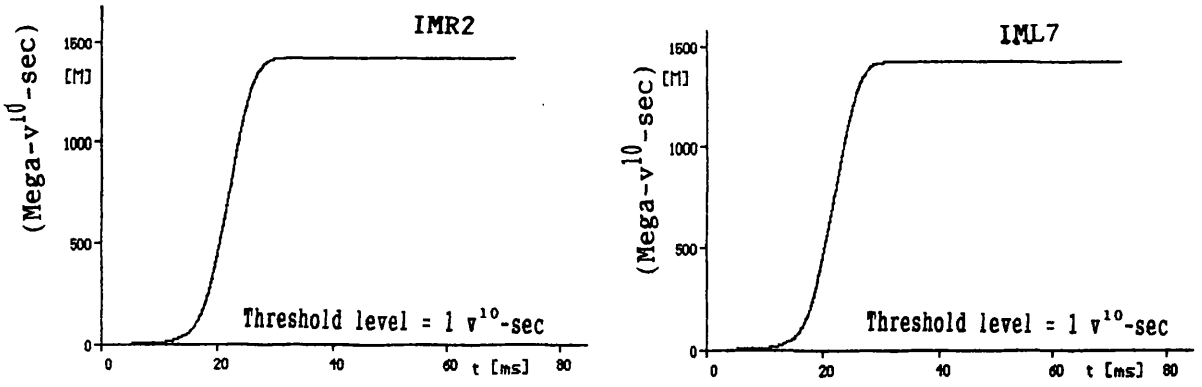


Figure 9.7 d
Signal processed signals from different stack tuners of figure 9.6 with r=10

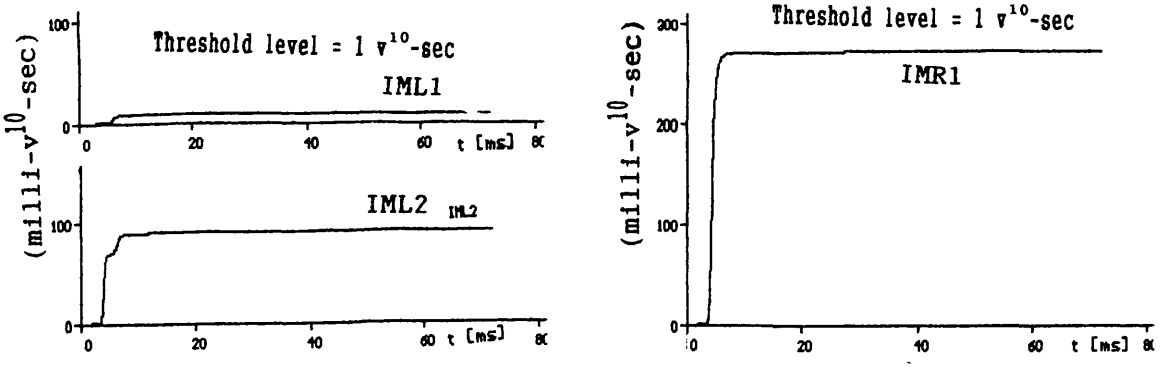


Figure 9.7 e
Expanded view of (invisiable) signals near zero magnitude in figure 9.7 d.

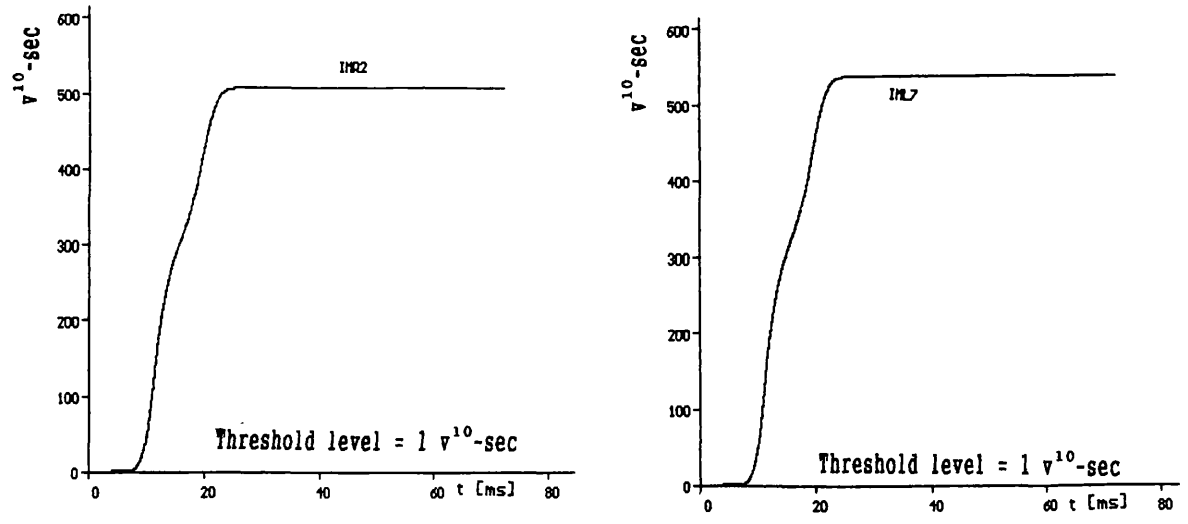


Figure 9.7 f
Modal raised integrated output for r=10, line to ground fault with fault resistance of 1000 ohms. All integrated outputs are near zero except IMR2 & IML7. The threshold level is (1 v^{10}-s).

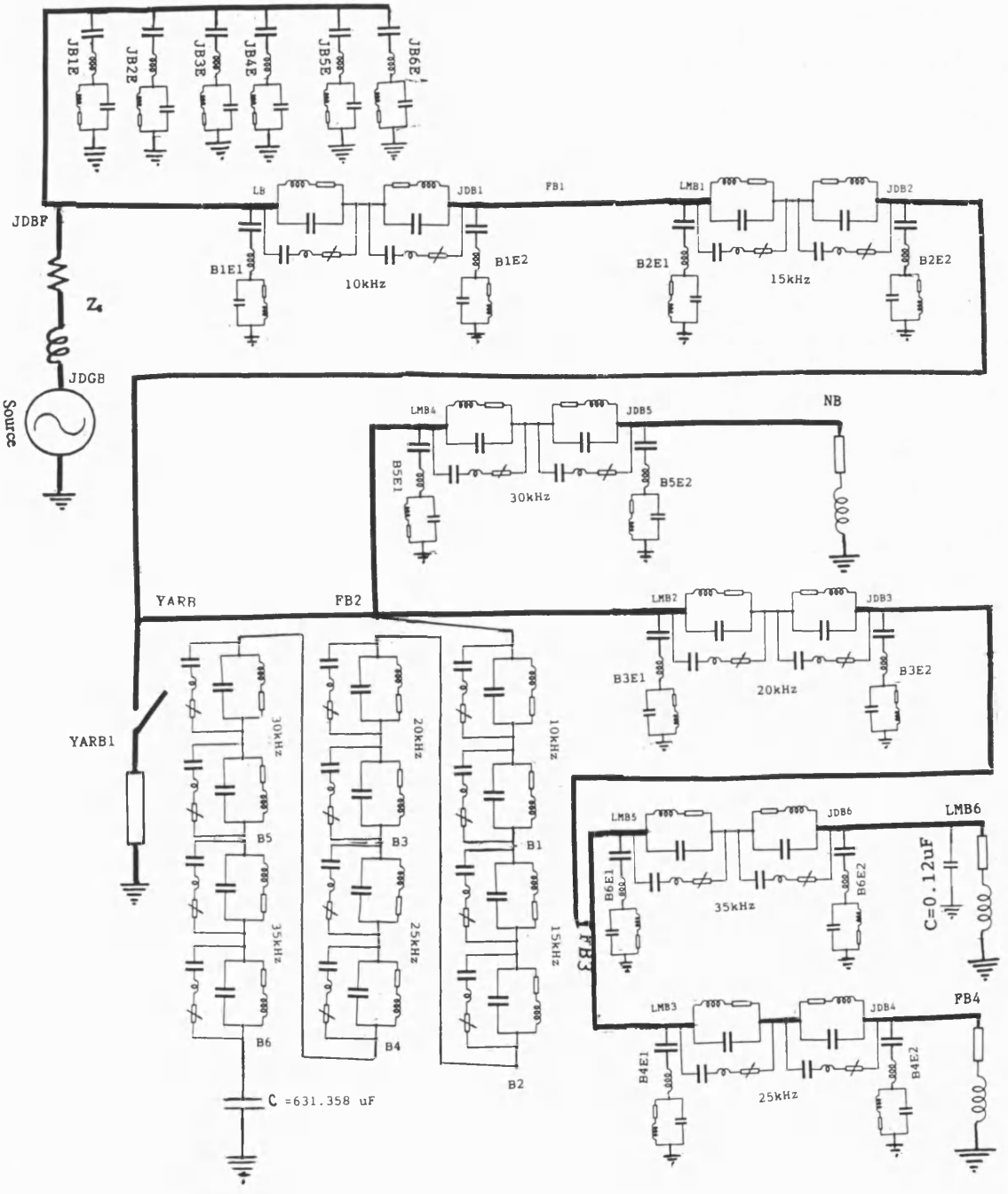


Figure 9.8 a (twin trap version)
Circuit arrangement of source-side-multi-frequency (remote) output type application of the fault locator.

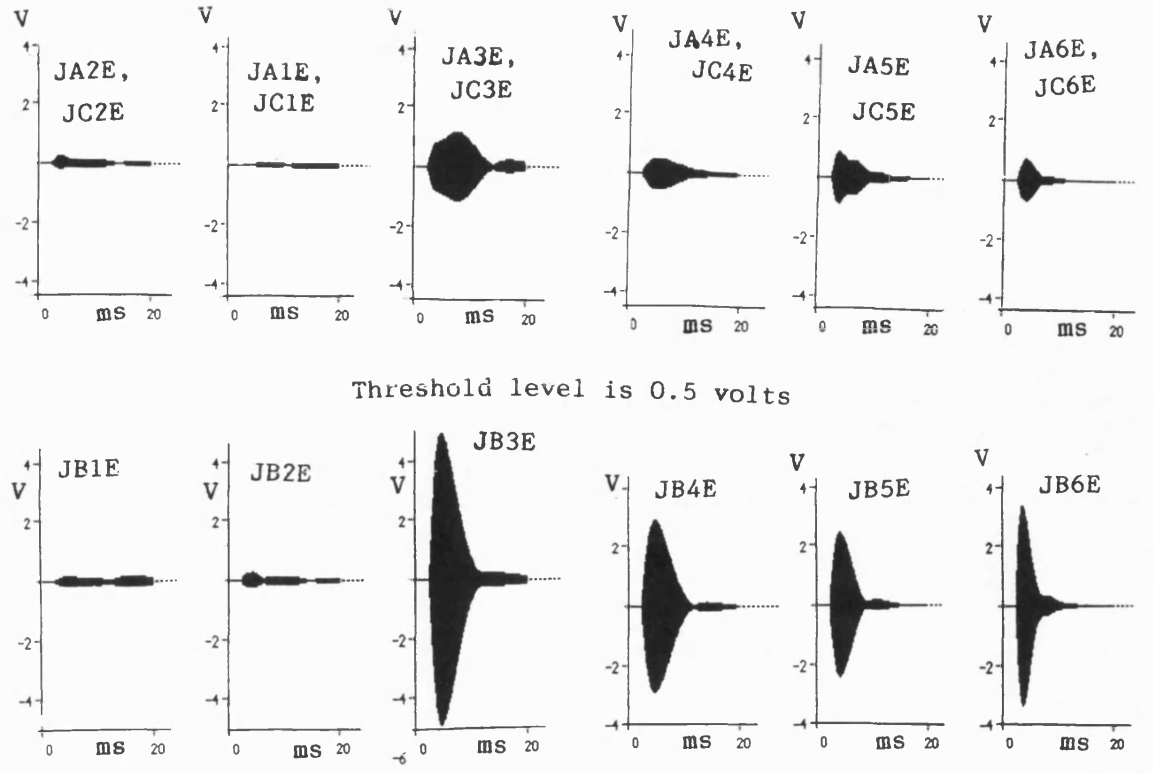


Figure 9.8 b (twin trap version)
Per phase signal outputs from fault locators with remote type application

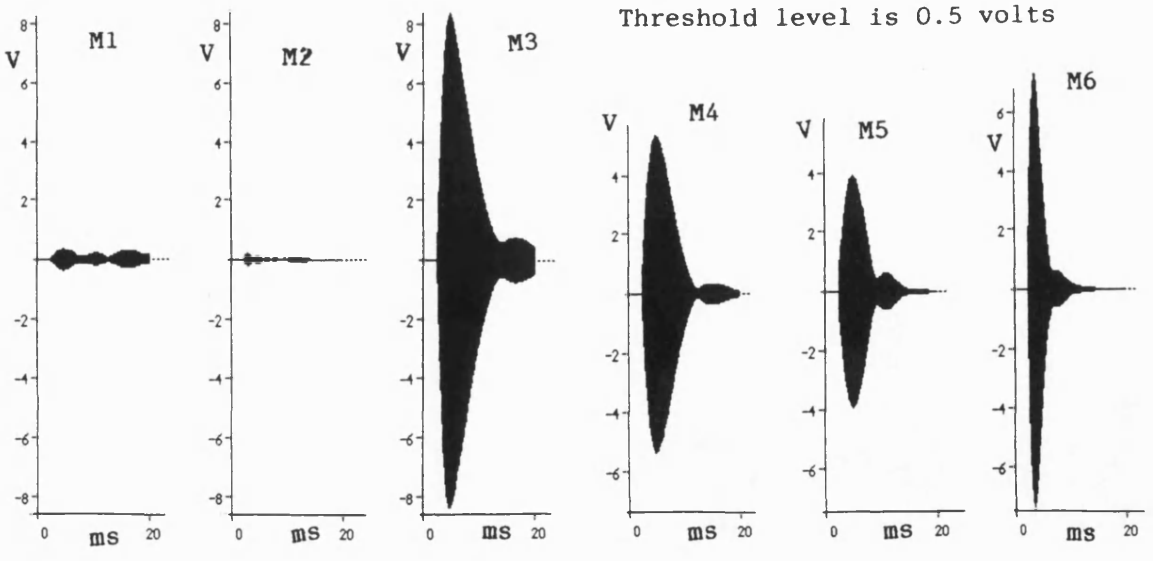


Figure 9.8 c (twin trap version)
Modal signal output voltages from fault locator with remote type application

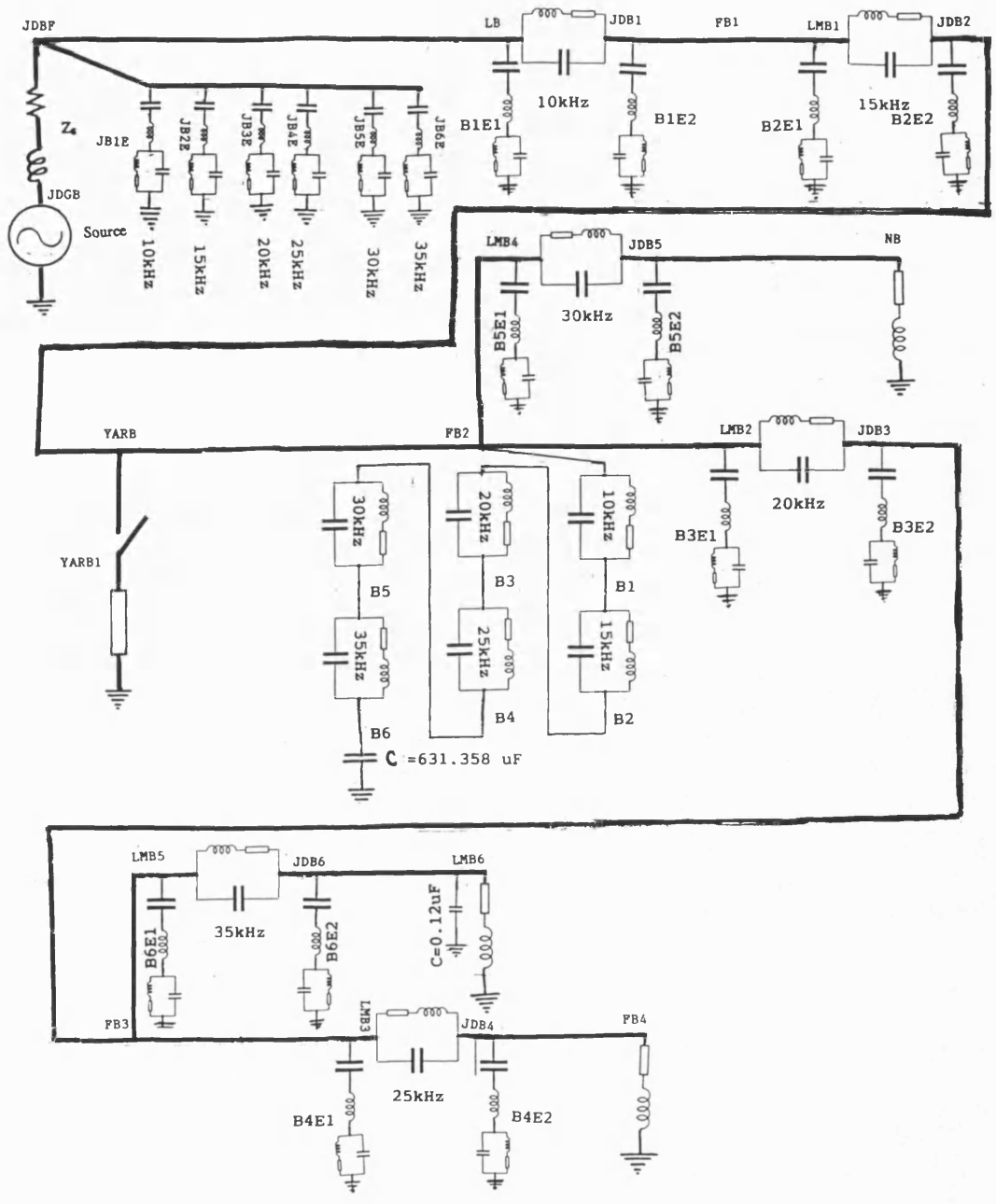


Figure 9.9 a (two-branch trap version)
Circuit arrangement of source-side-multi-frequency (remote) output type application of the fault locator.

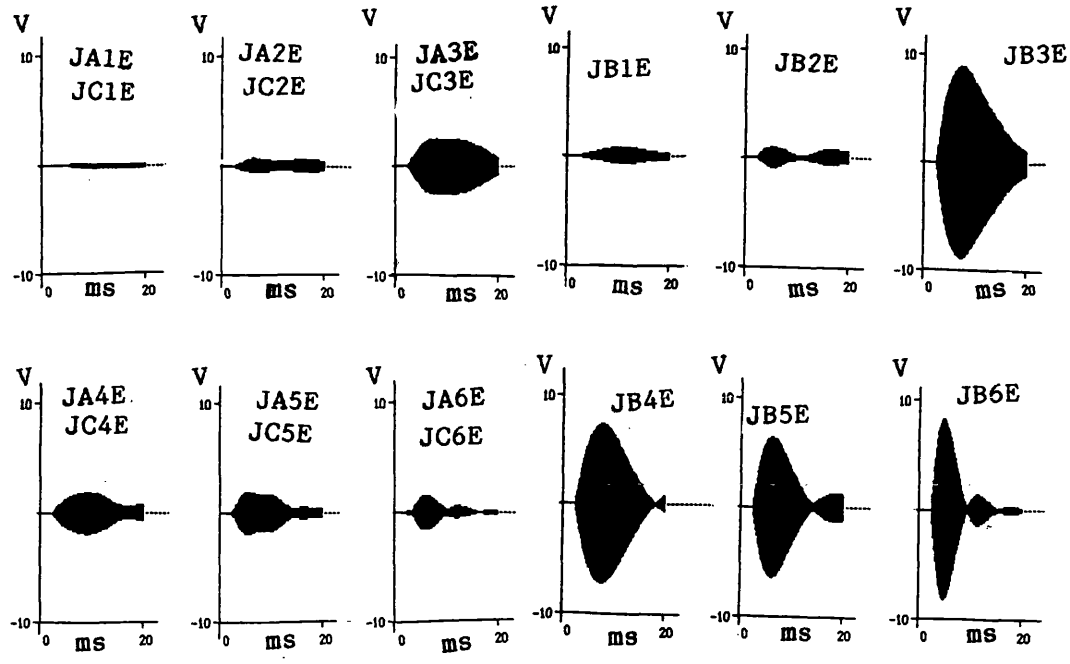


Figure 9.9 b (two-branchrap version)
Per phase signal outputs from fault locators with remote type application

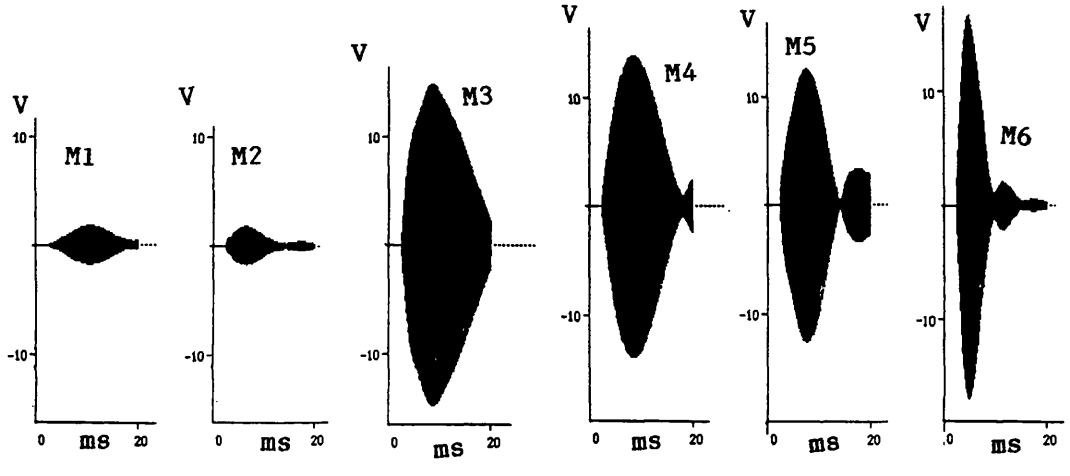


Figure 9.9 c (two-branch trap version)
Modal signal output voltages from fault locator with remote type application

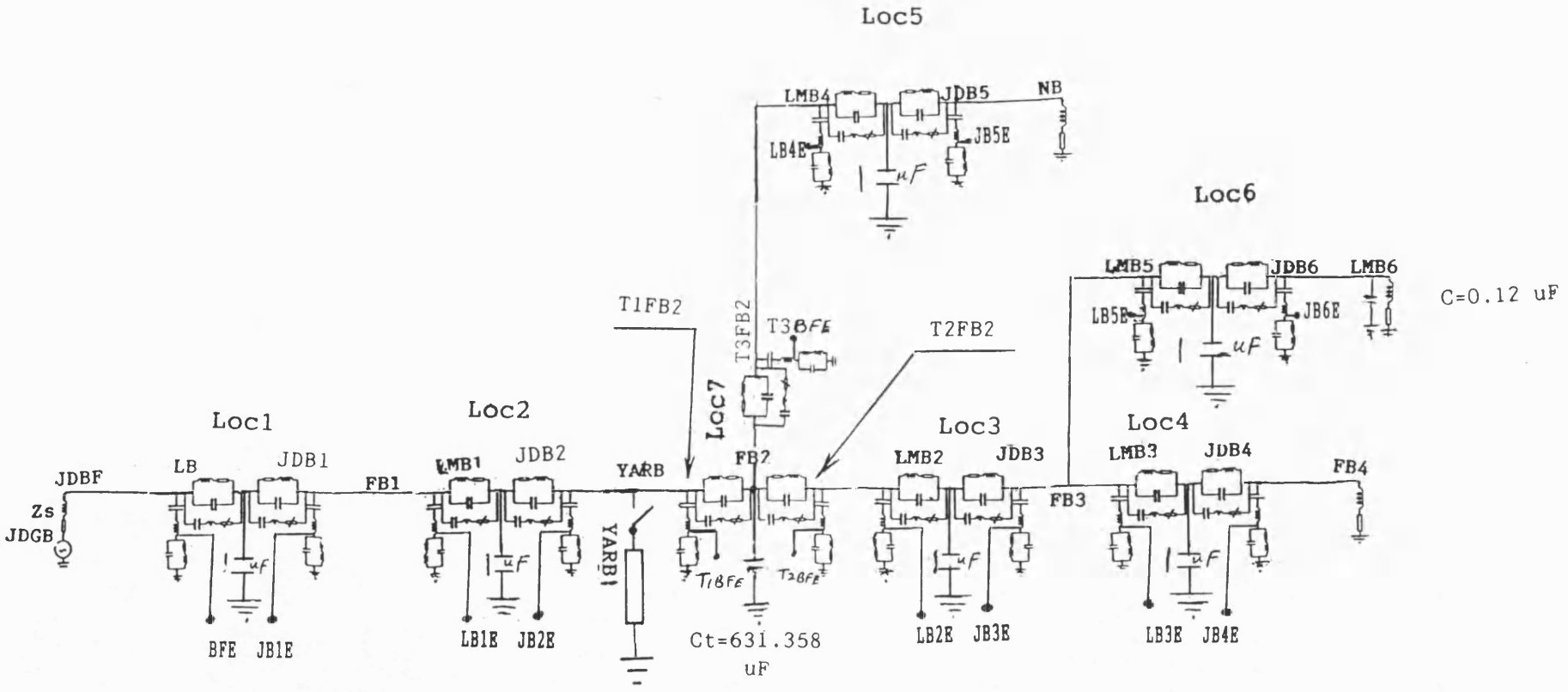


Figure 9.10 a
Circuit arrangement to study universal application of the fault locator

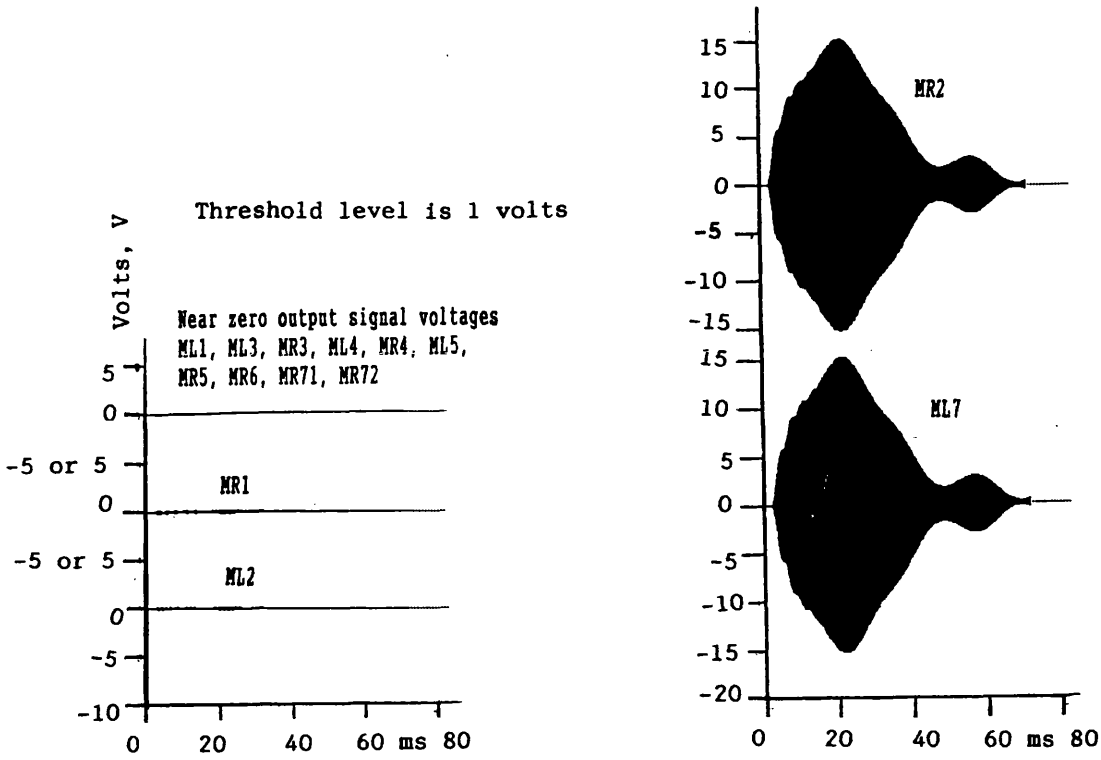


Figure 9.10 b (Solid earth fault)
Modal output voltages from universal type application of the fault locator

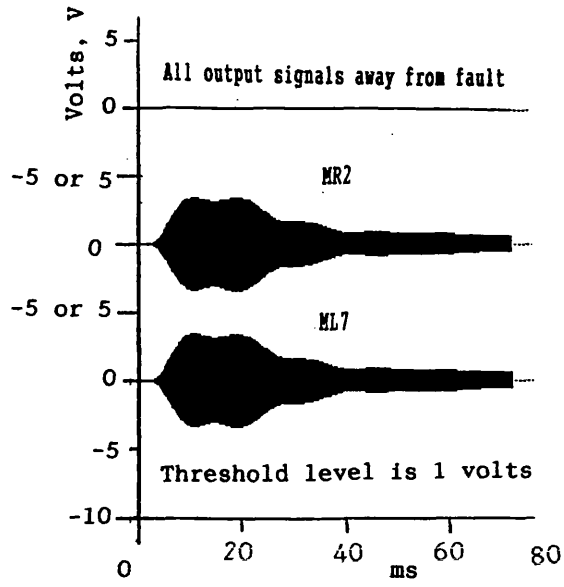
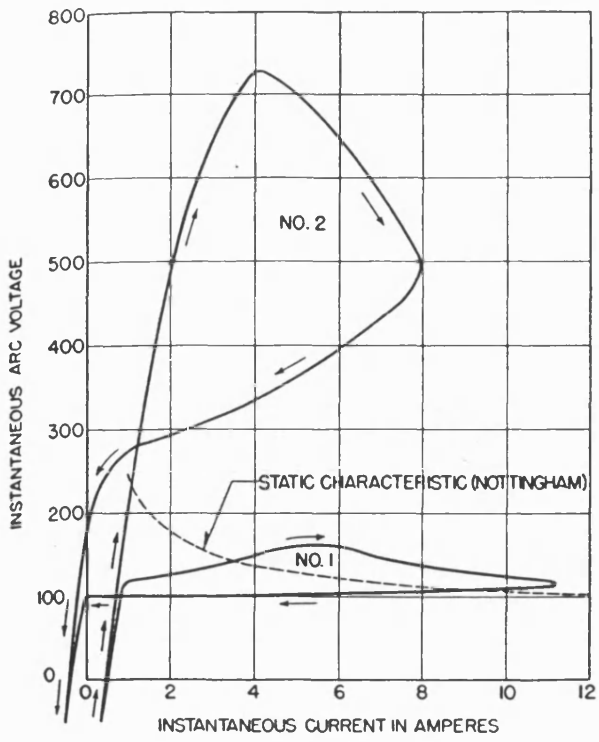
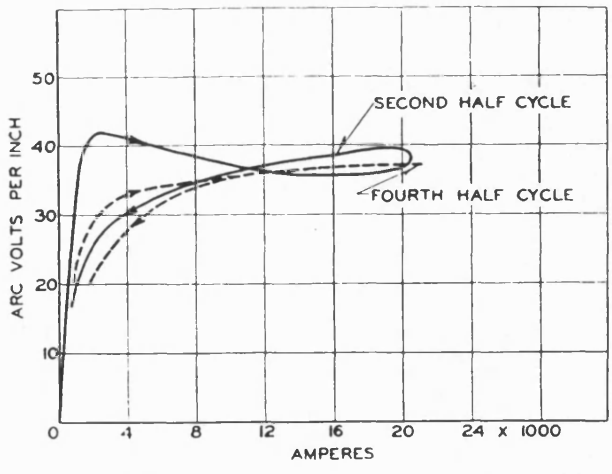


Figure 9.10 C (through fault resistance of 1000 ohms)
Modal output voltages from universal type application of the fault locator



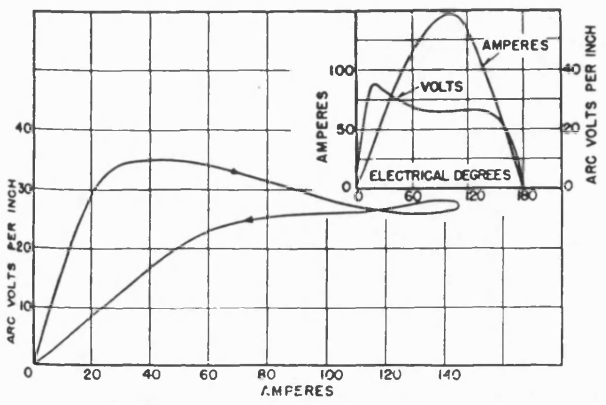
Volt-ampere cyclograms of 60-cycle arcs in air between copper electrodes 1.5 in. apart. No. 1, arc still about 1.5 in. long; No. 2, arc lengthened by convection almost to breaking point.

Figure 10.1
This figure is taken from the work of Browne of ref. 48



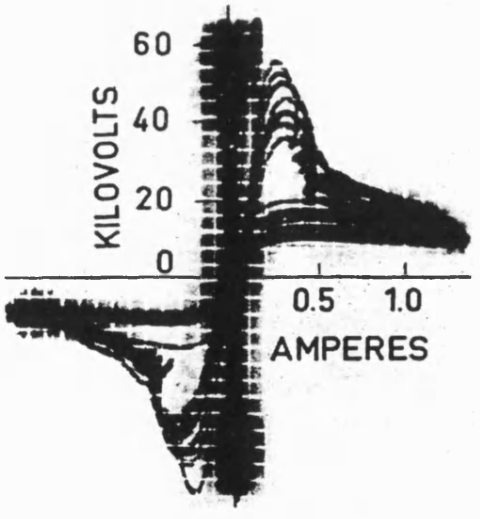
Volt-ampere cyclograms of vertical 60-cycle arc 12 in. long in air, 15,000 amp rms.

Figure 10.2
This figure is taken from the work of Browne of ref. 48



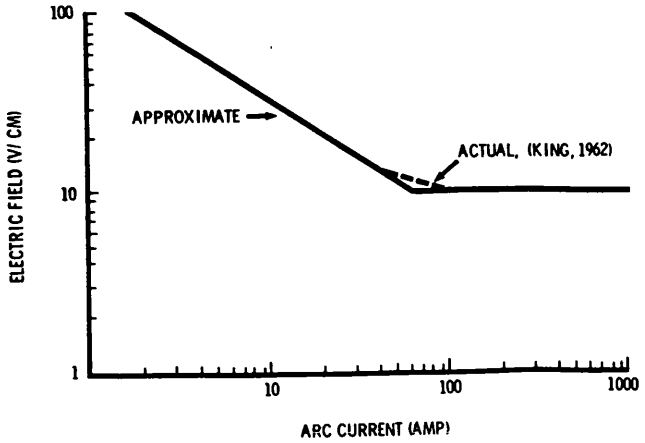
Volt-ampere cyclogram of vertical 60-cycle arc 48 in. long in air, 100 amp rms.

Figure 10.3
This figure is taken from the work of Browne of ref. 48
It shows experimental work of Strom [49].



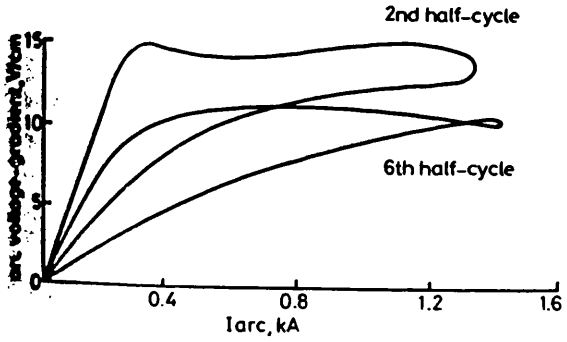
Cathode-ray volt-ampere cyclogram of vertical 60-cycle arc drawn to a length of 48 in. in a 40-kv circuit in air.

Figure 10.4
This figure is taken from the work of Browne of ref. 48



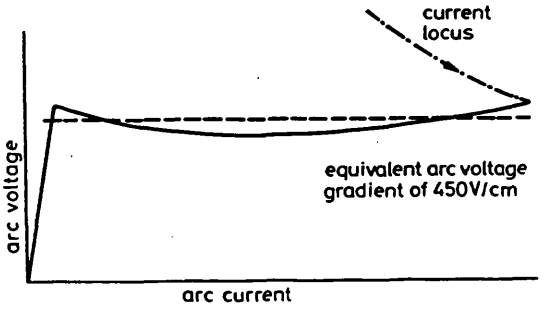
Volt-ampere characteristics for long, free vertical air arcs.

Figure 10.5
This figure is taken from the work of Latham of ref. 52



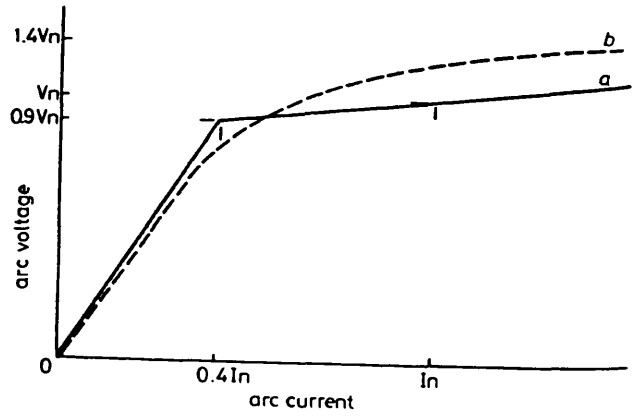
Characteristics of heavy-current power arcs

Figure 10.6
This figure is taken from the work of Cornick of ref.53



Characteristics of weak-current power arcs

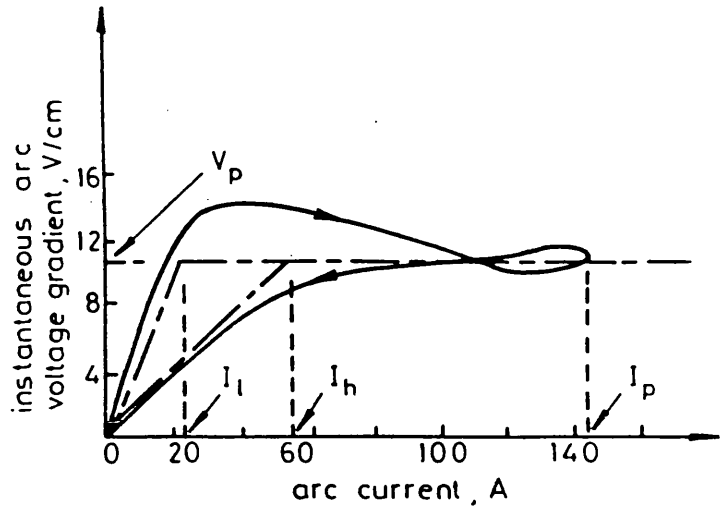
Figure 10.7
This figure is taken from the work of Cornick of ref.53



Normalised arcing-fault characteristic

a piecewise
b modified 7th order

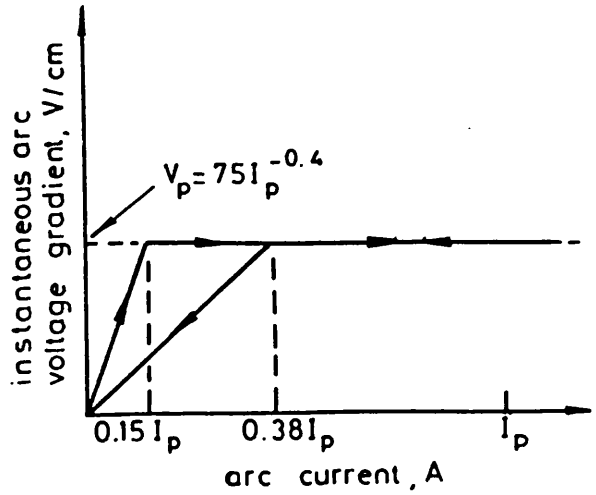
Figure 10.8
This figure is taken from the work of Cornick of ref.53



Typical long arc cyclogram

$I_l \simeq 21$ A $\simeq 0.15\,I_p$; $I_n \simeq 55$ A $\simeq 0.38\,I_p$; $I_p \simeq 144$ A; $V_p \simeq 10.3$ V;
characteristic repeated for negative halfcycle
——— actual cyclogram
— — — piecewise-linear approximation

Figure 10.9
This figure is taken from the work of Johns & Al-Rawi of ref.56



Normalised linearised arc cyclogram

Characteristic repeated for negative halfcycle

Figure 10.10
This figure is taken from the work of Johns & Al-Rawi of ref.56

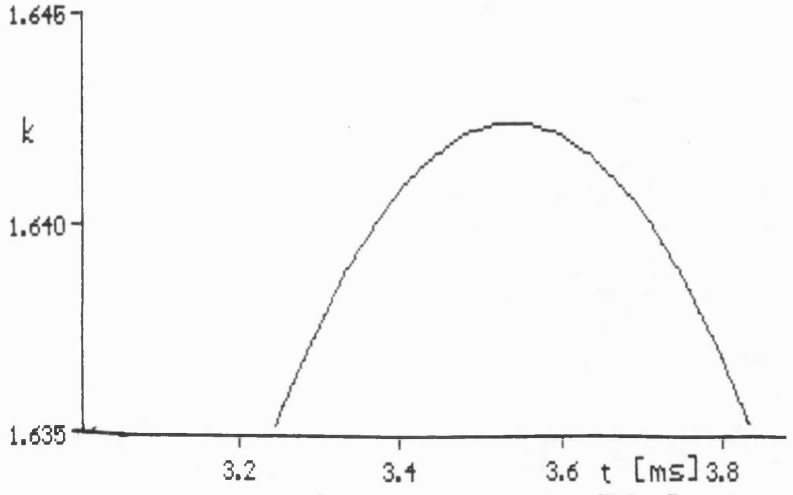


Figure 10.11
Determination of peak value I_p of steady-state fault current from simulation test by short circuiting arcing nodes.

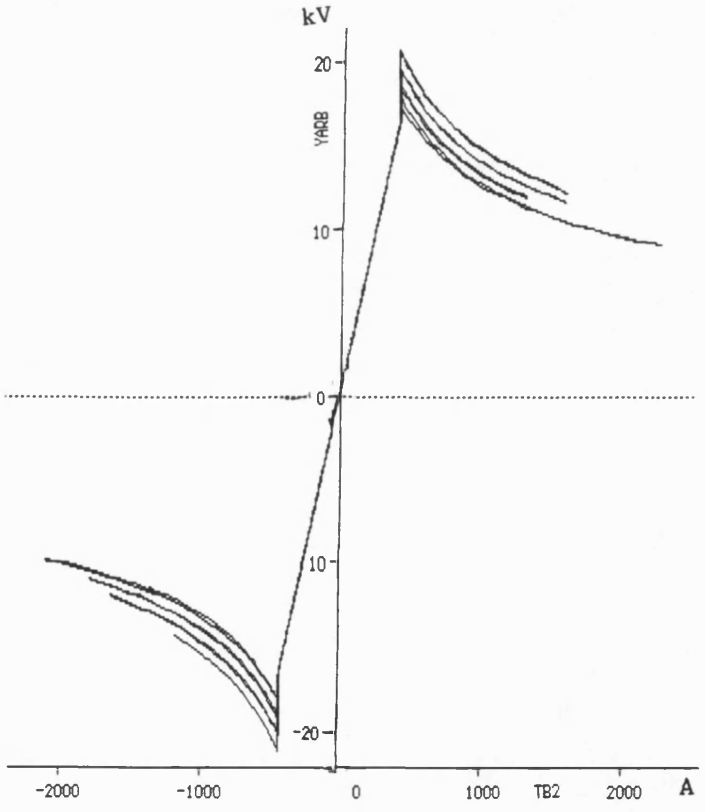


Figure 10.12
Cyclogram of present arc fault across 500 cm air gap for arc voltage YARB versus arc current TB2.

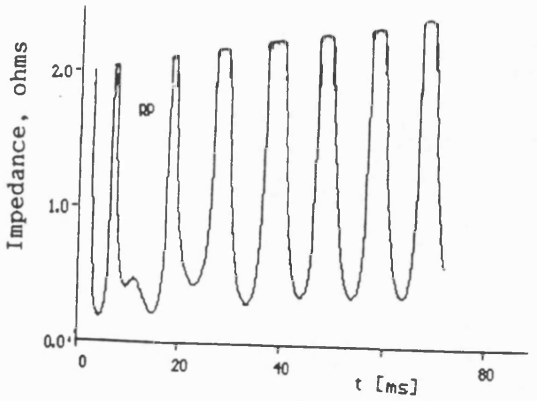


Figure 10.13
Arc fault resistance across 500 cm airgap.

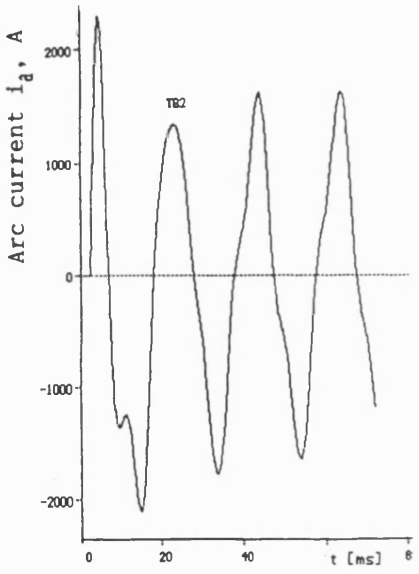


Figure 10.14
Arc fault current from the
moment of arc initiation
to the moment of arc extinction.

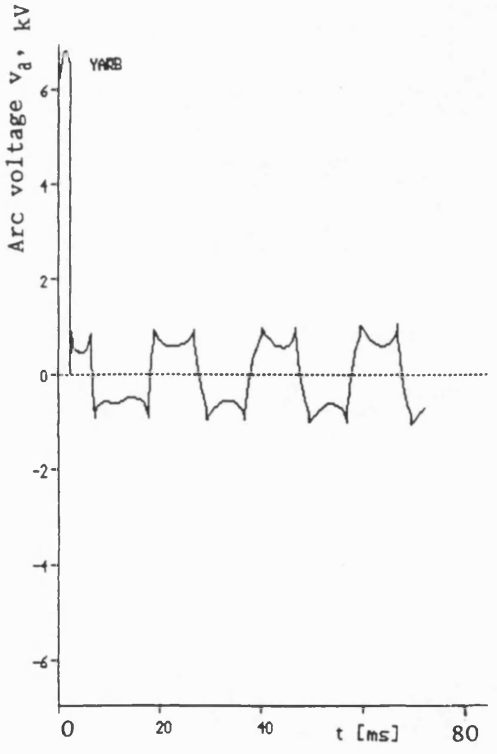


Figure 10.15
arc voltage across airgap of
500 cm on phase-B at YARB.

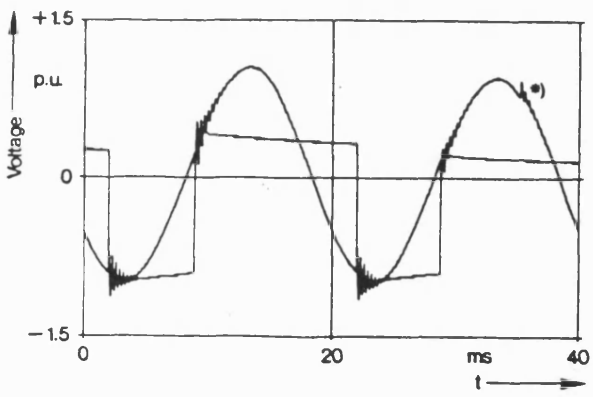


Figure 61 — Low frequency transients, interaction between phases * — Busbar length on load side 20 m.

Figure 10.16
Experimental arc voltages taken from ref. 62

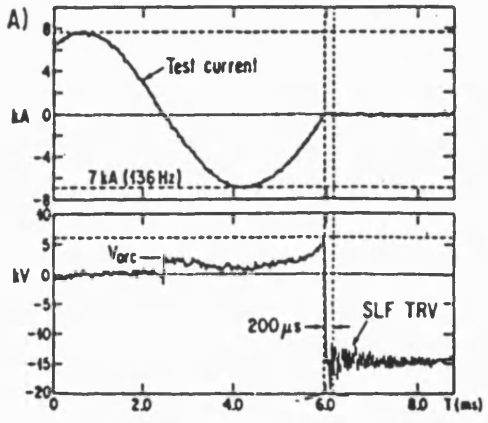


Figure 10.17
Experimental arc voltages and currents taken from ref. 62.

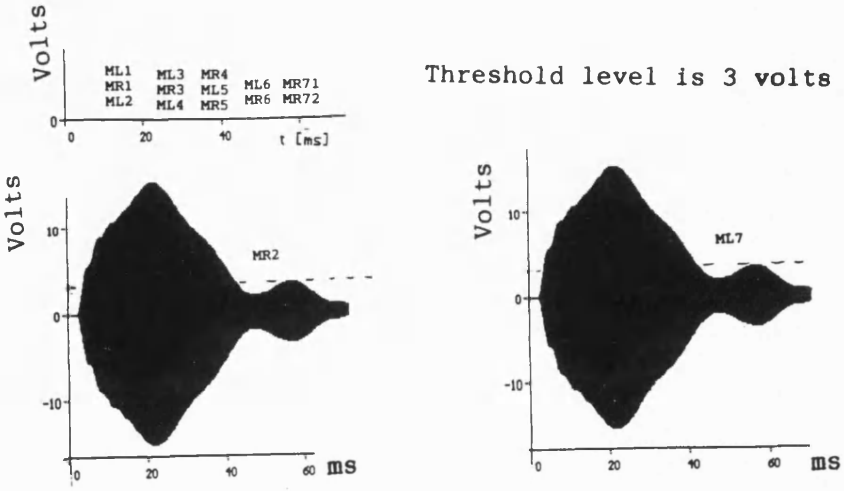


Figure 10.18
Modal form output signal voltages at 10 kHz.

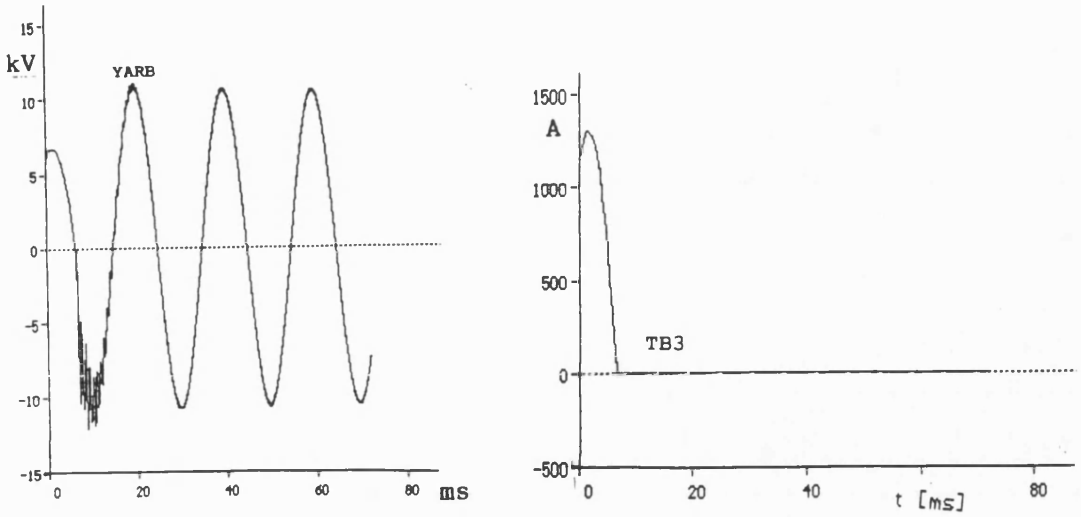


Figure 11.1
Open phase fault (a) per phase voltage YARB & (b) line current TB3

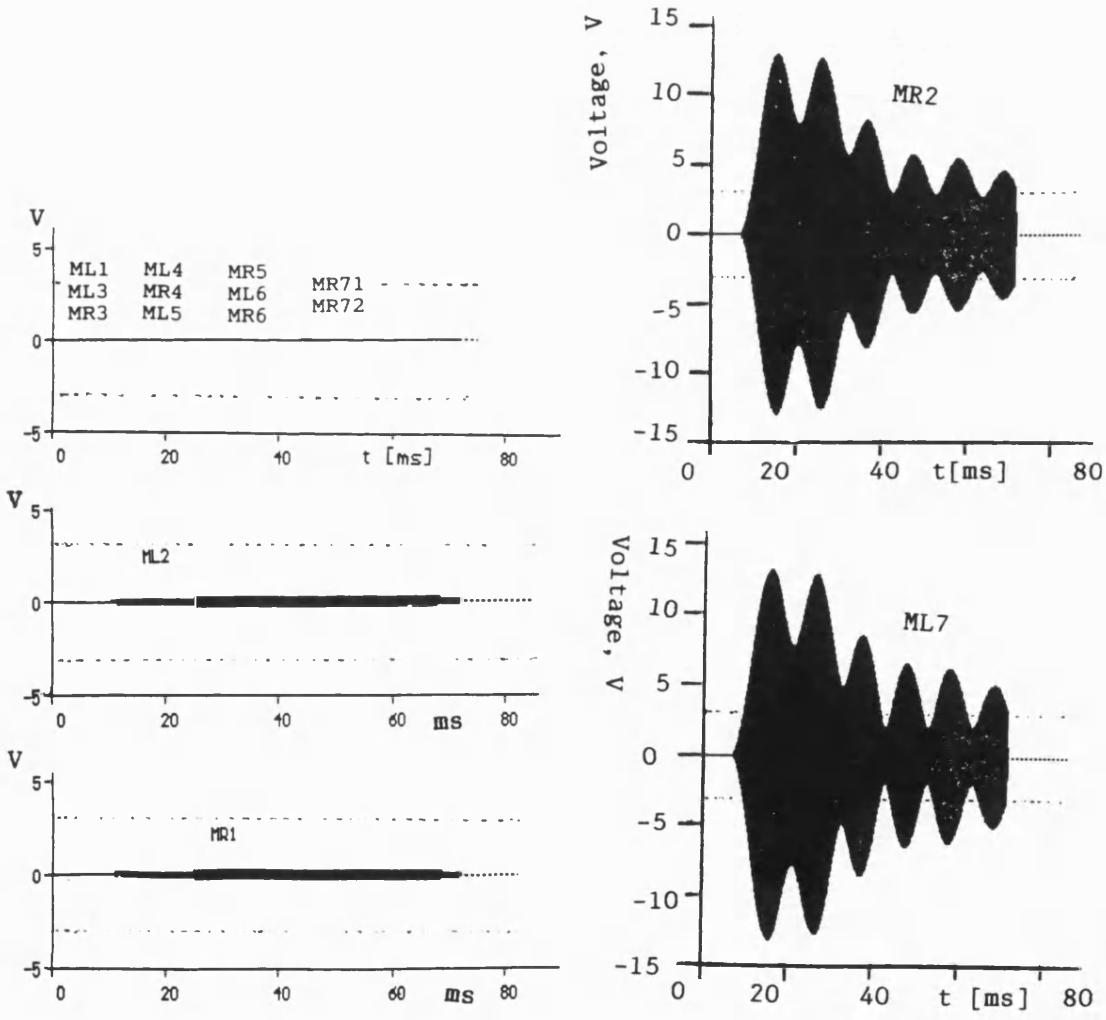


Figure 11.2
Performance of the fault locator during open phase fault.

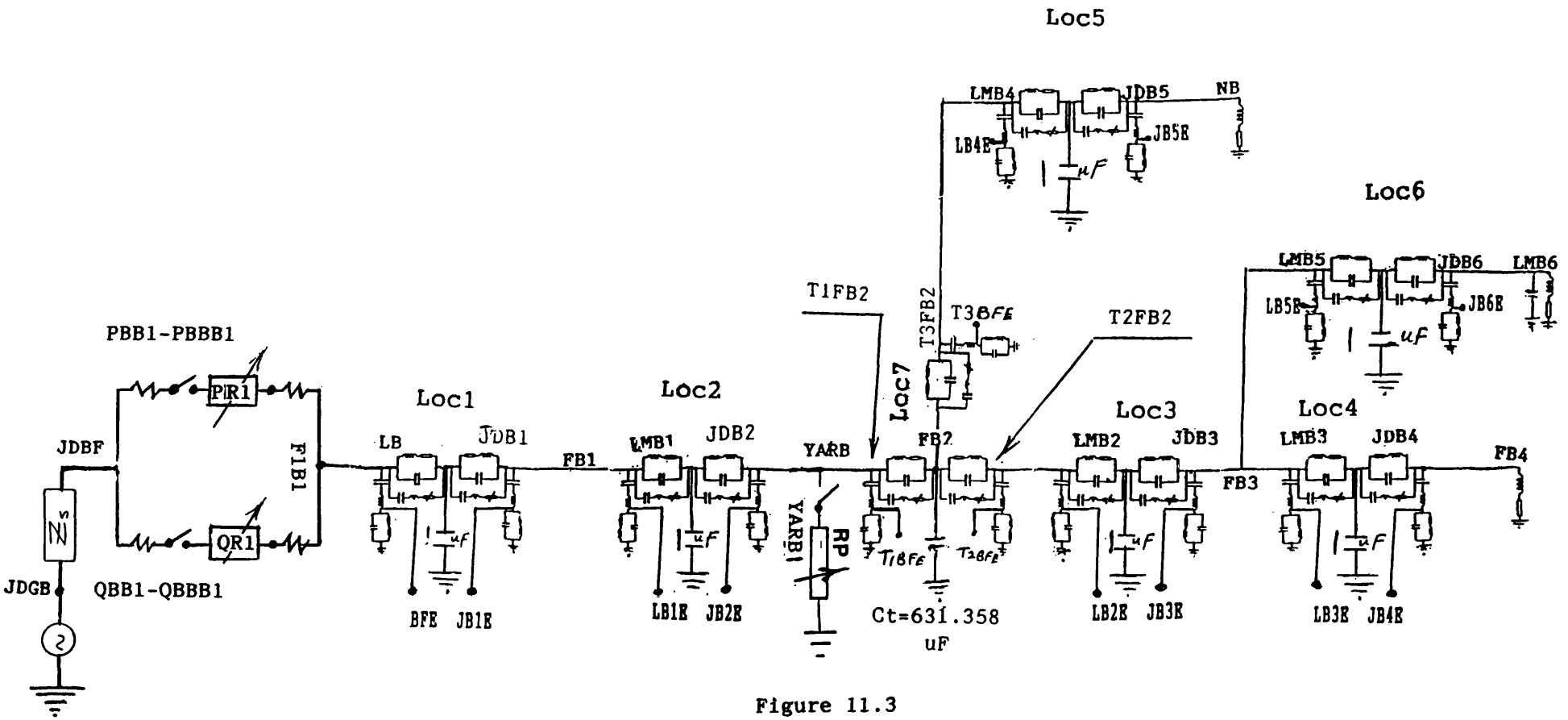


Figure 11.3

phase-B circuit arrangement of the 11kV system

for the circuit breaker arc simulation and line to earth arc

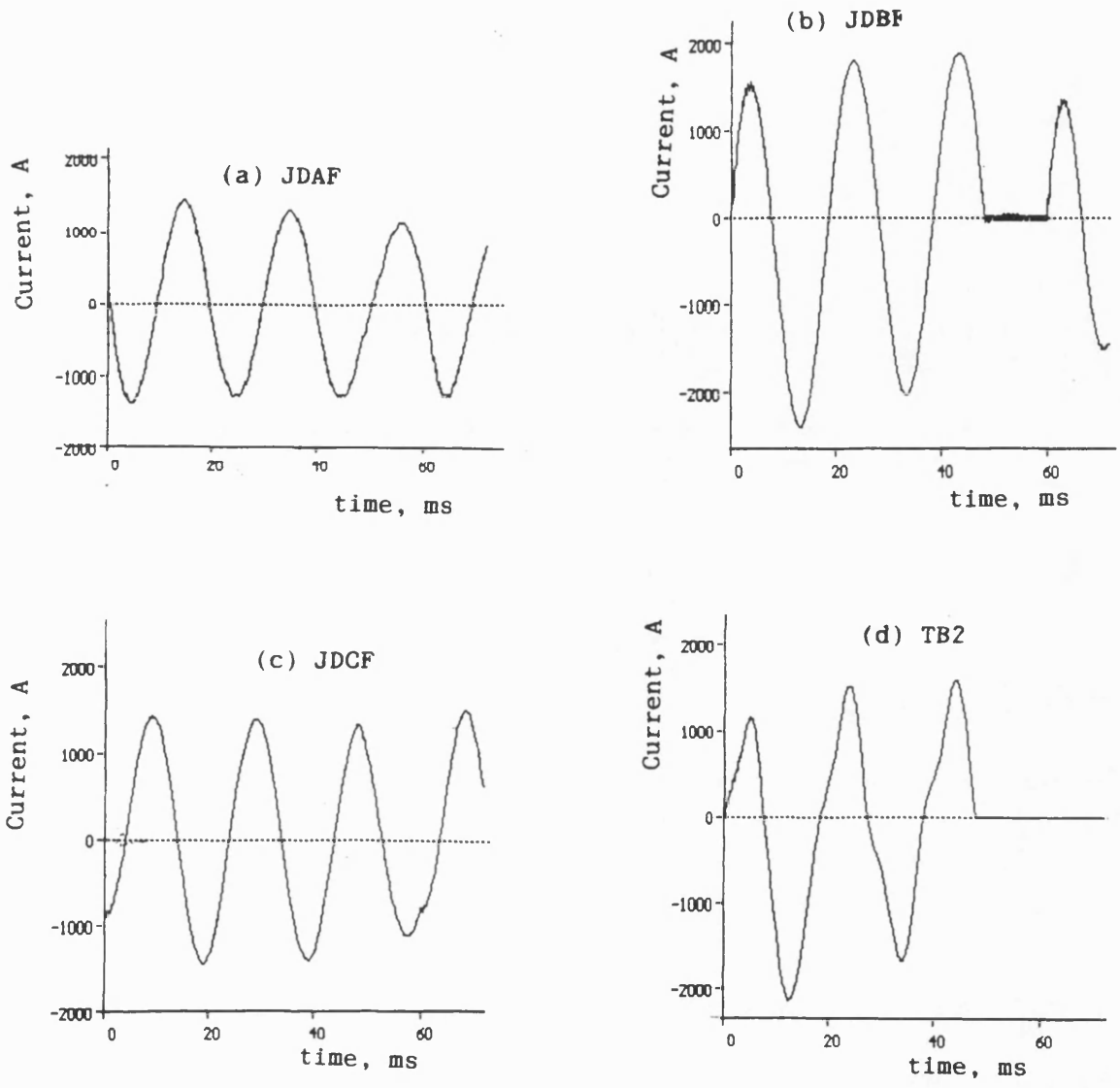


Figure 11.4
Currents at various nodes of the 11 kV network, during arcing fault.

and circuit breaker operation

(a) current of a-phase
(b) current of b-phase i.e. fault current
(c) current of c-phase
(d) current to earth at fault point

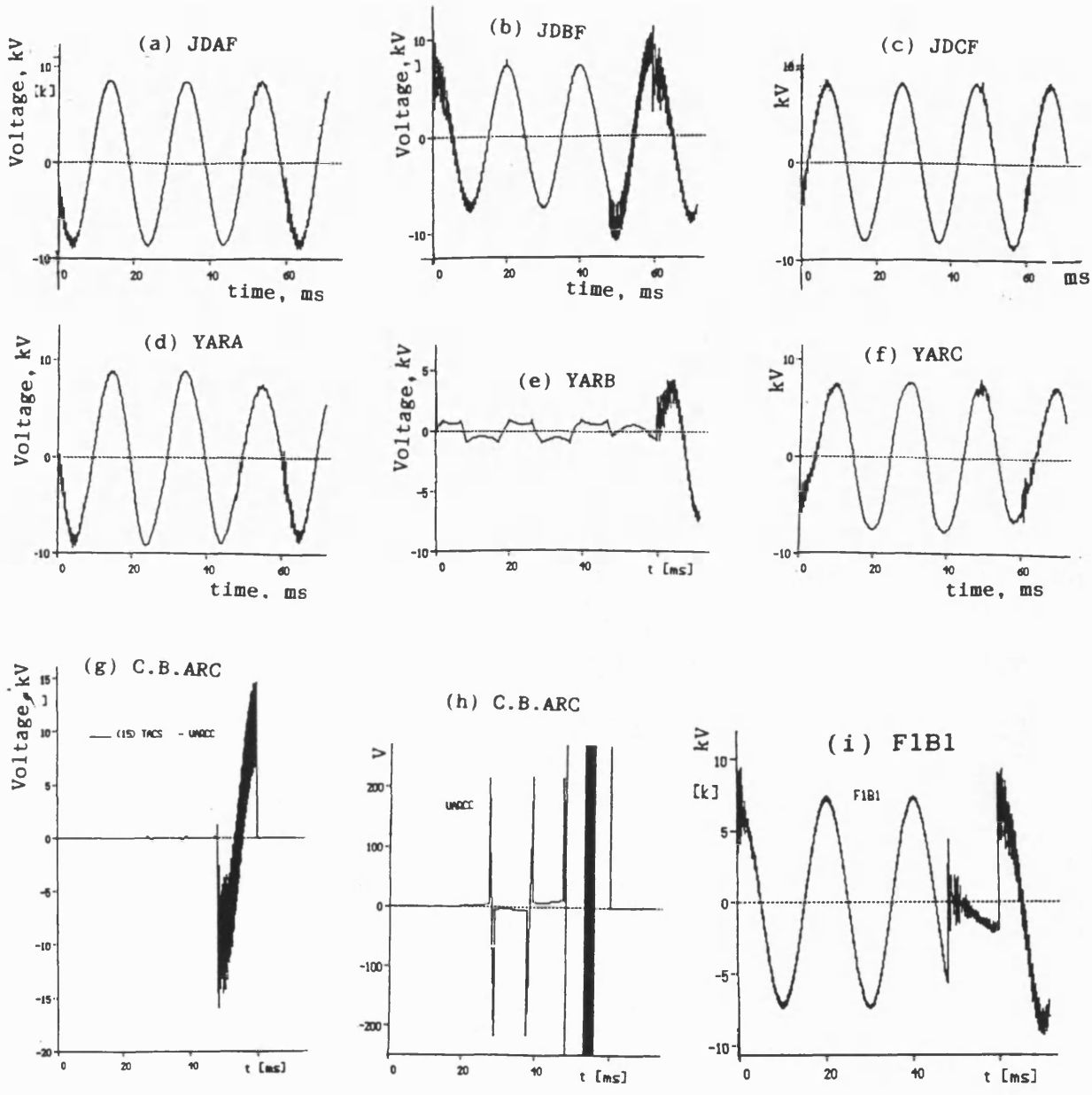


Figure 11.5
Voltages at various nodes of the 11 kV network during arcing earth fault and circuit breaker operation

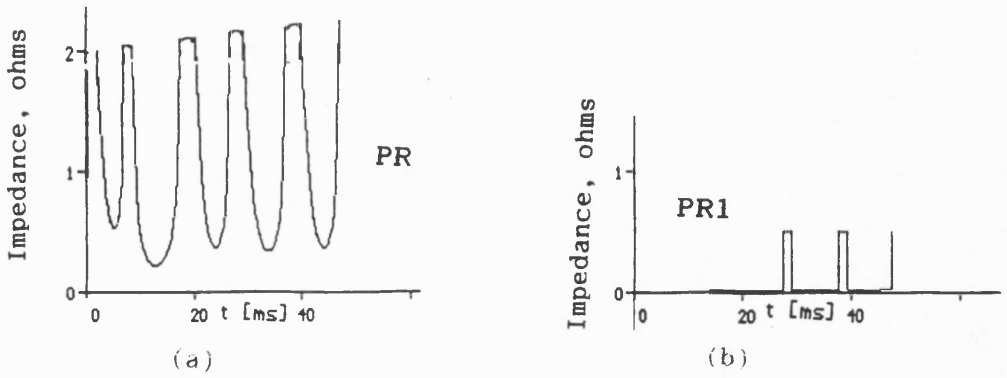


Figure 11.6
Arc resistances, arcing earth fault resistance Rp and arcing circuit breaker resistance PR1 during periods of arcing.

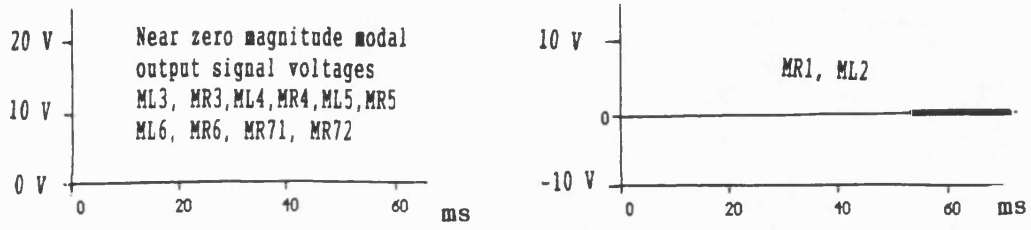


Figure 11.7
Fault locator output during arcing fault and circuit breaker operation

Signal output voltages from stack tuners away from earthing earth fault

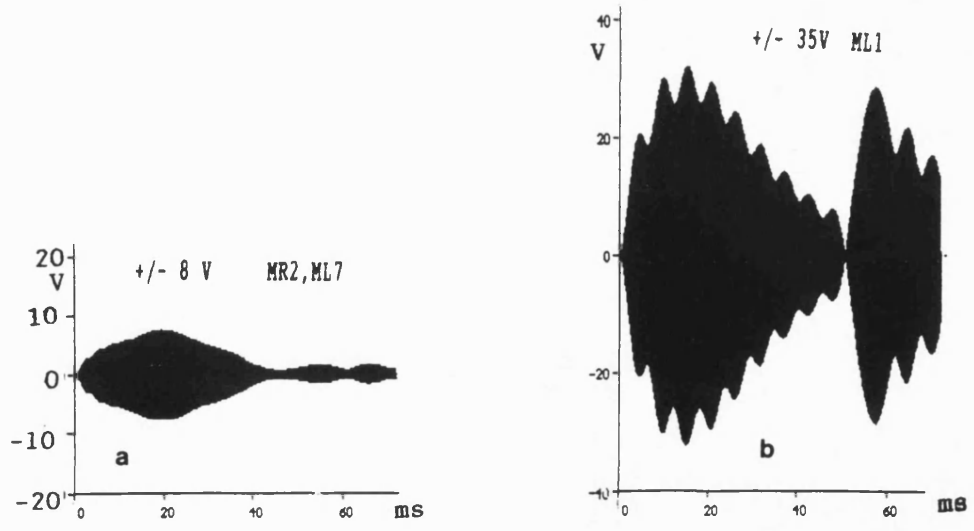


Figure 11.7
Fault locator output during arcing fault and circuit breaker operation

(a) Signal output voltages from stack tuners close & on both sides of arcing earth fault

(b) Signal output voltages from stack tuners close & on both sides of operating circuit breaker

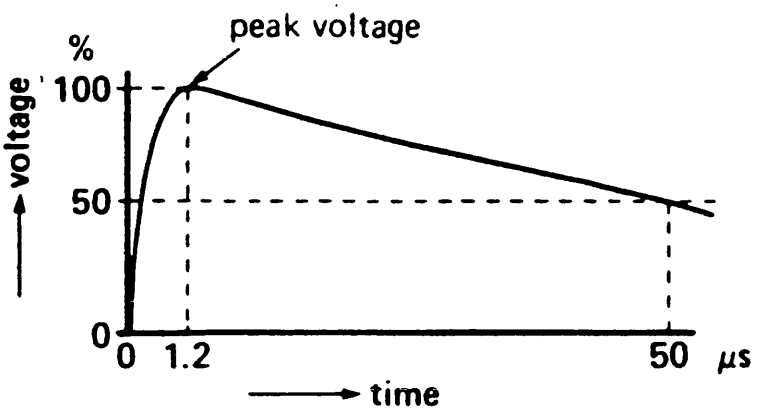


Figure 12.1 Standard shape of impulse voltage used to determine the BIL rating of electrical apparatus.

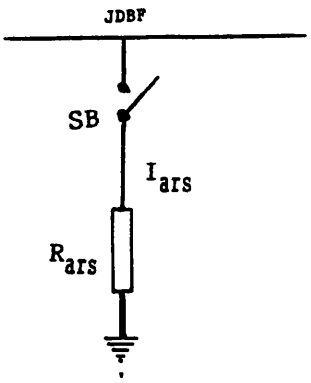


Figure 12.2
Basic circuit arrangement of a non-linear resistance for EMTP

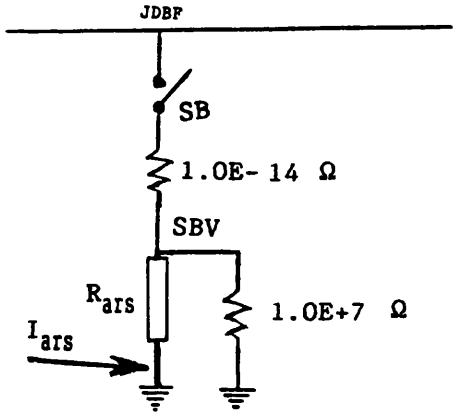


Figure 12.3
Non-linear modal for surge arrestor

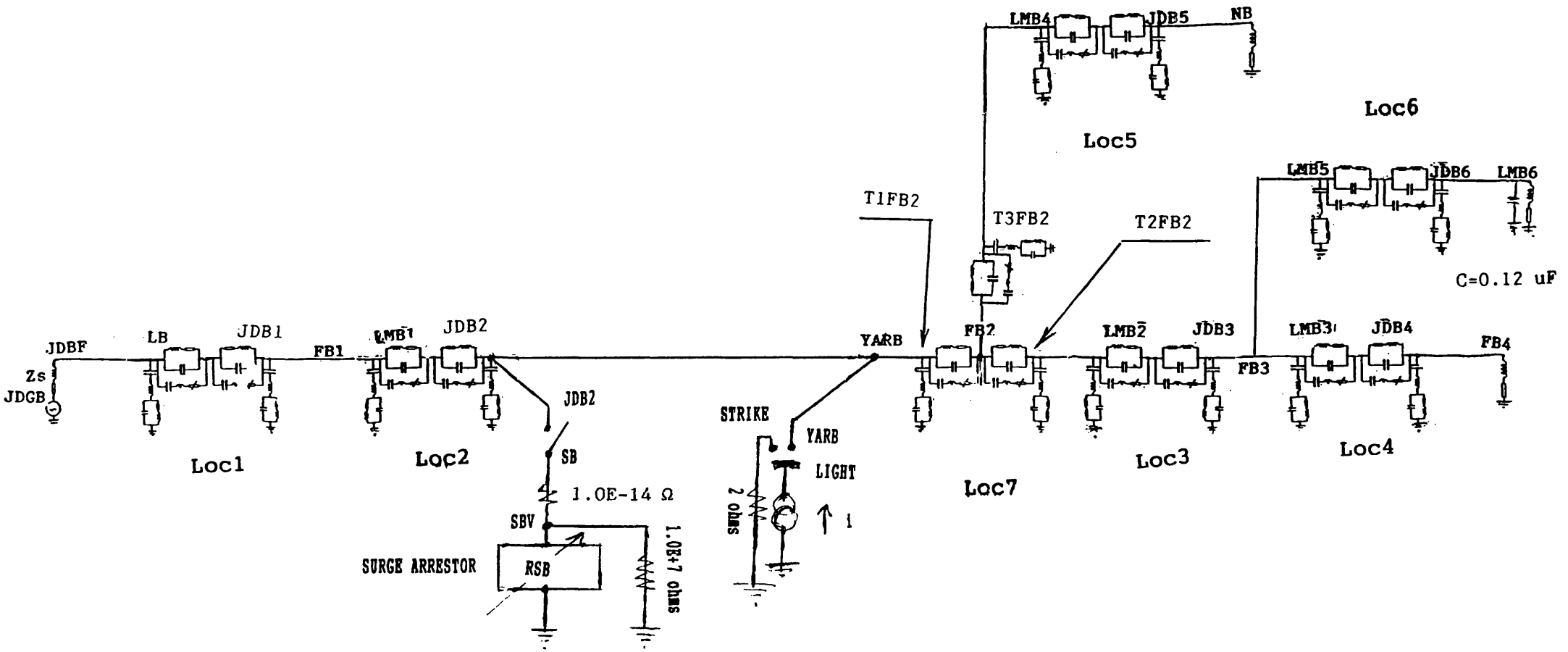


Figure 12.4
Circuit arrangement to study effect of Lightning
on fault locator performance and safety

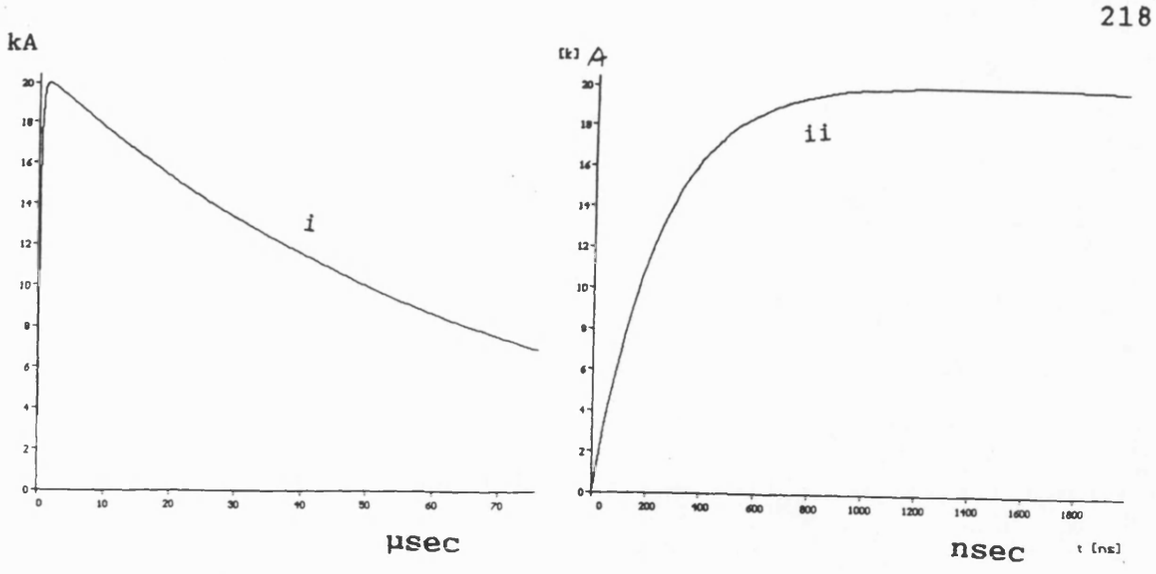


Figure 12.5 a
Lightning current impulse for present simulation
(i) Impulse for complete duration of simulation
(ii) Impulse expanded for first 2 micro seconds

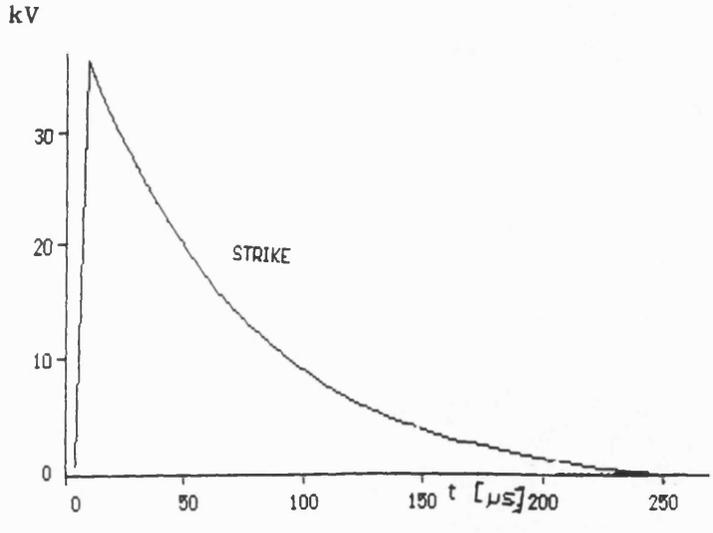


Figure 12.5 b
Lightning voltage created after hitting of lightning stroke on a 2 ohms pole

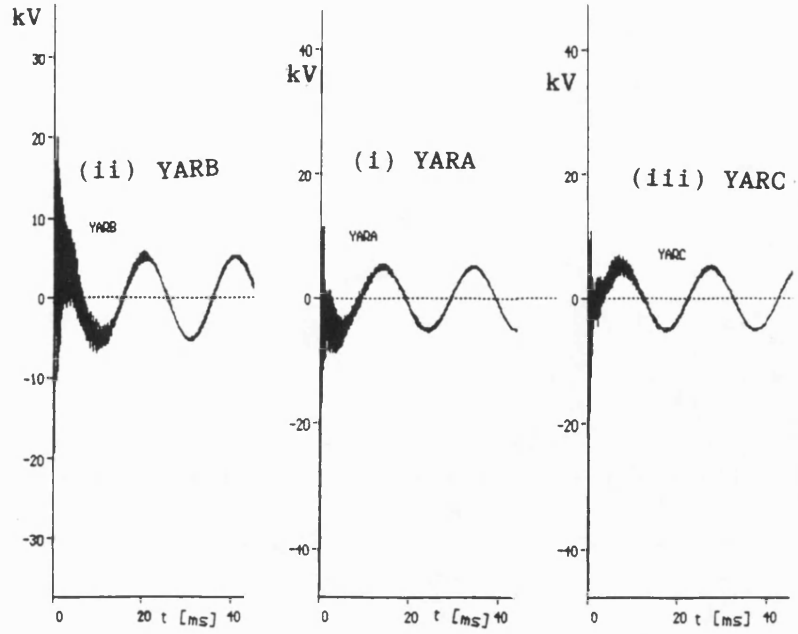


Figure 12.6 a
Voltage at striking nodes YARA, YARB and YARC

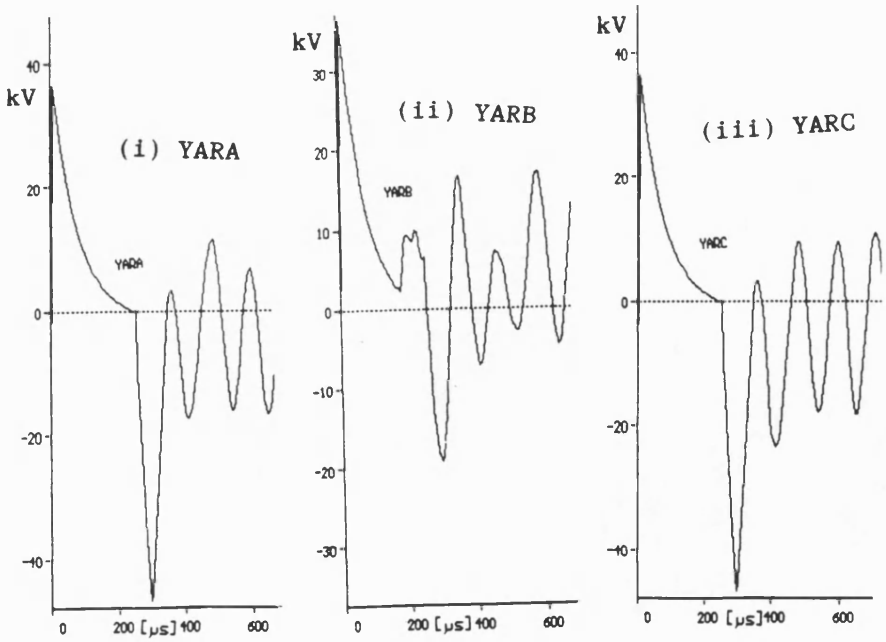


Figure 12.6 b
Expanded view of figure 12.6 a

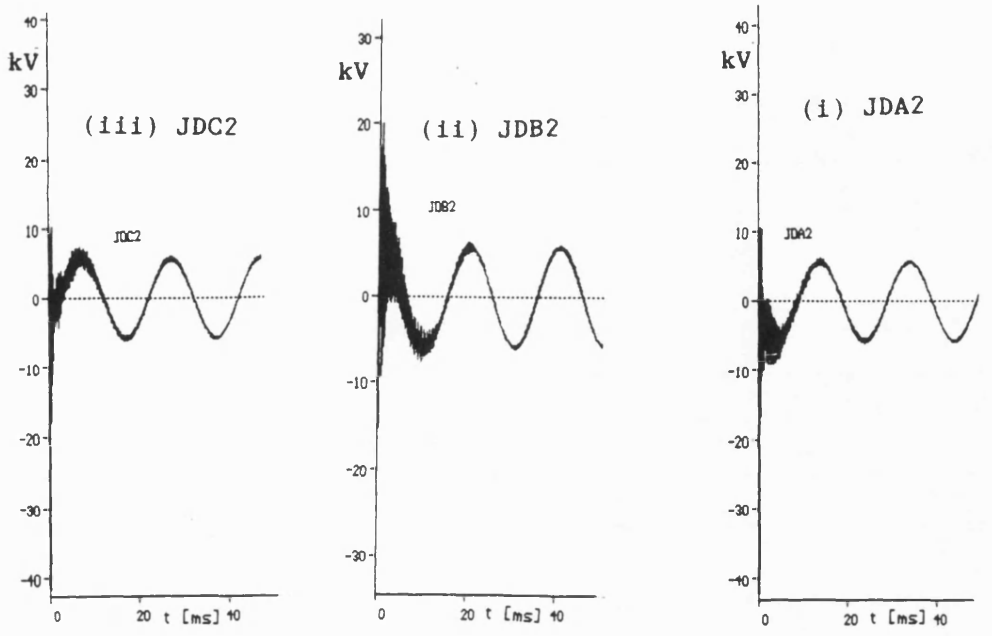


Figure 12.7 a
Voltages at nodes JDA2, JDB2 & JDC2

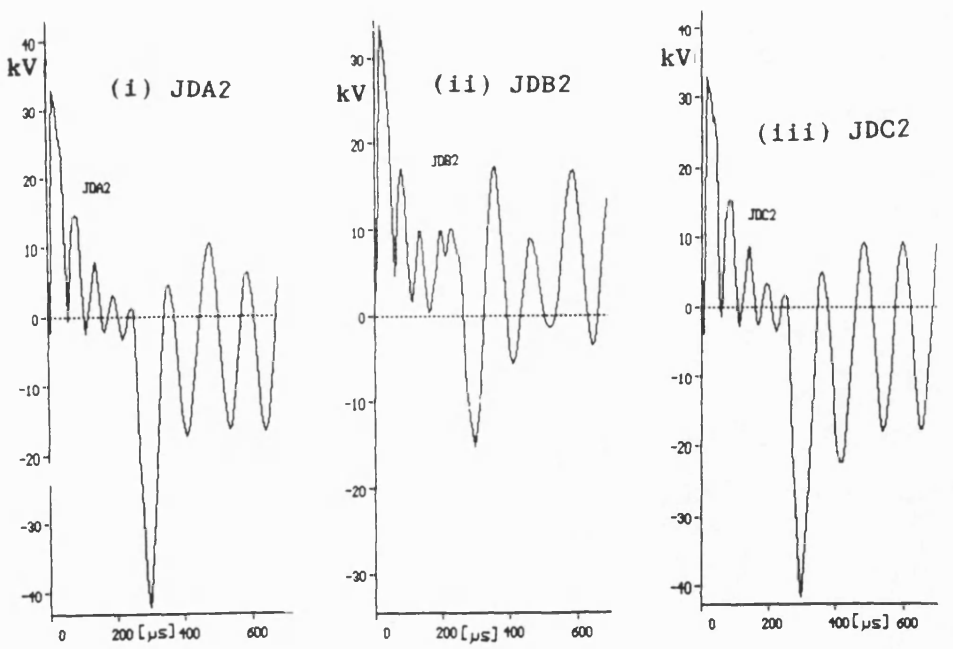


Figure 12.7 b
Expanded view of figure 12.7 a

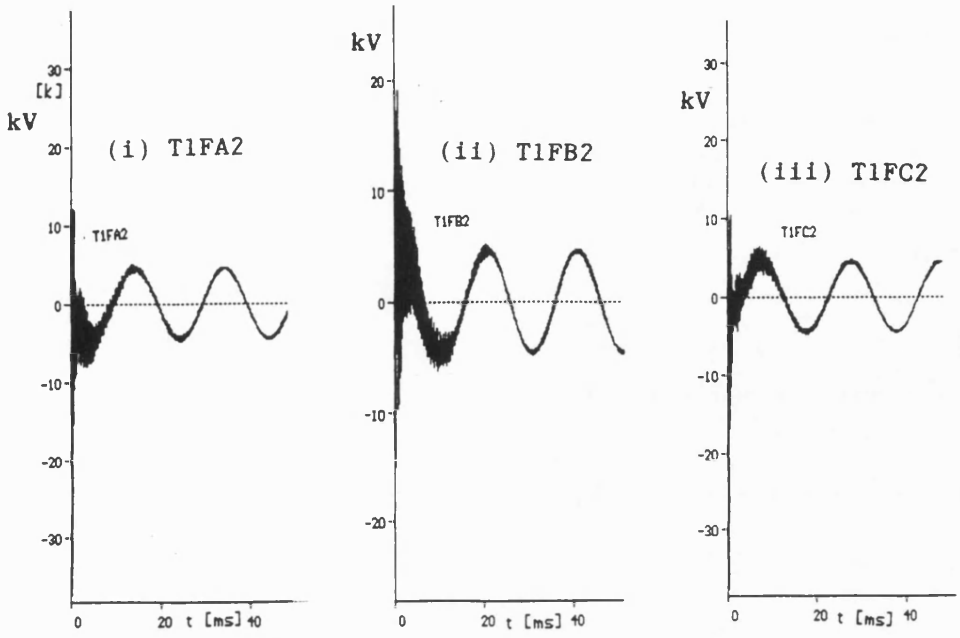


Figure 12.8 a
Voltages at T1FA2, T1FB2 and T1FC2

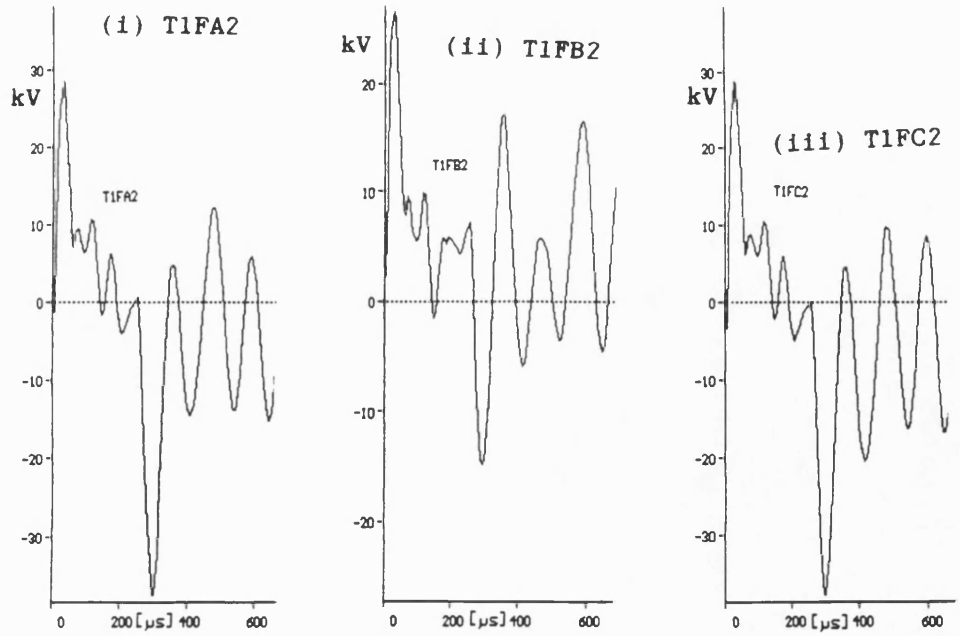


Figure 12.8 b
Expanded view of figure 12.8a

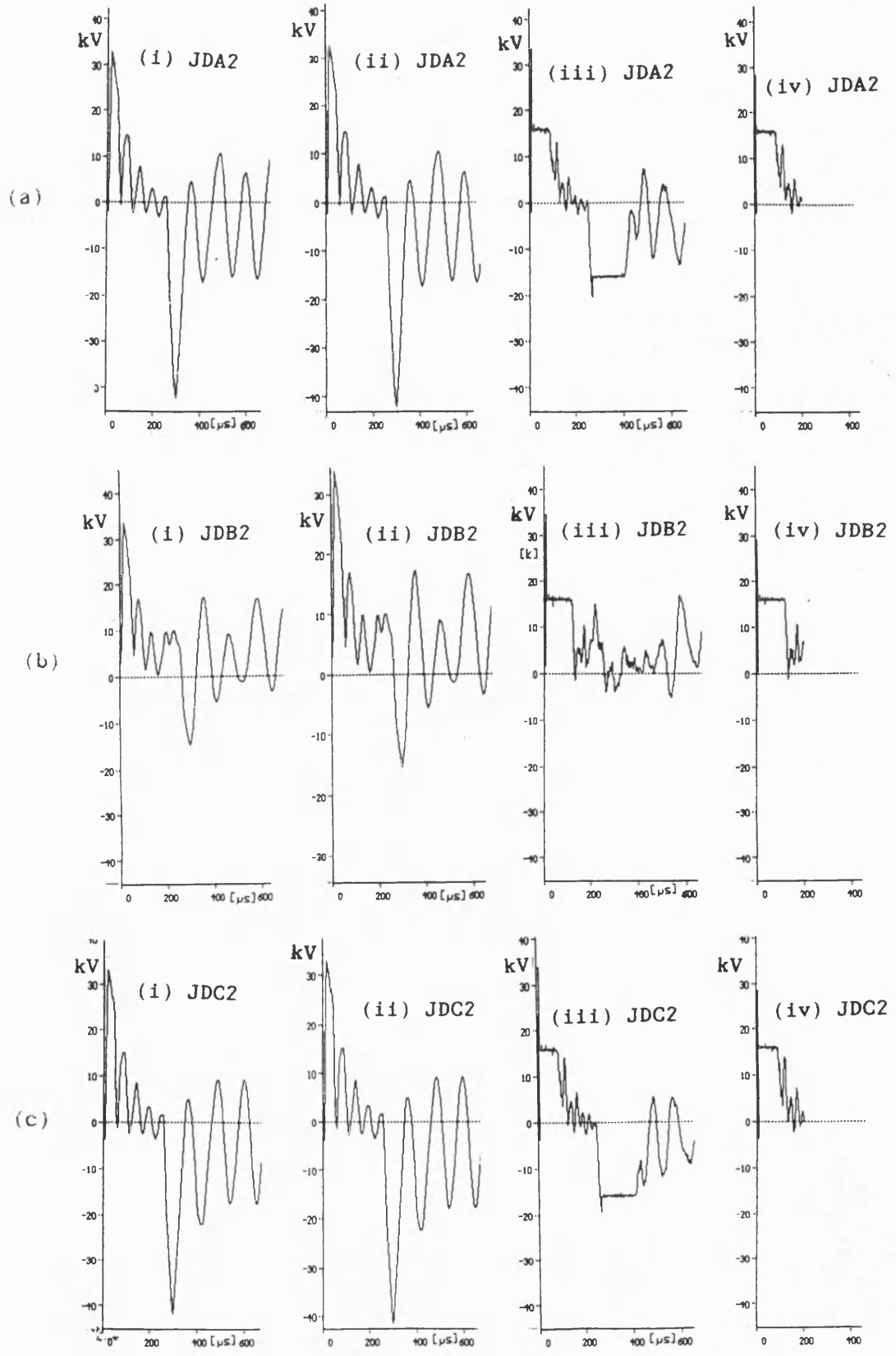


Figure 12.9
Voltages across surge arrester at nodes (a) JDA2, (b) JDB2 & (c) JDC2

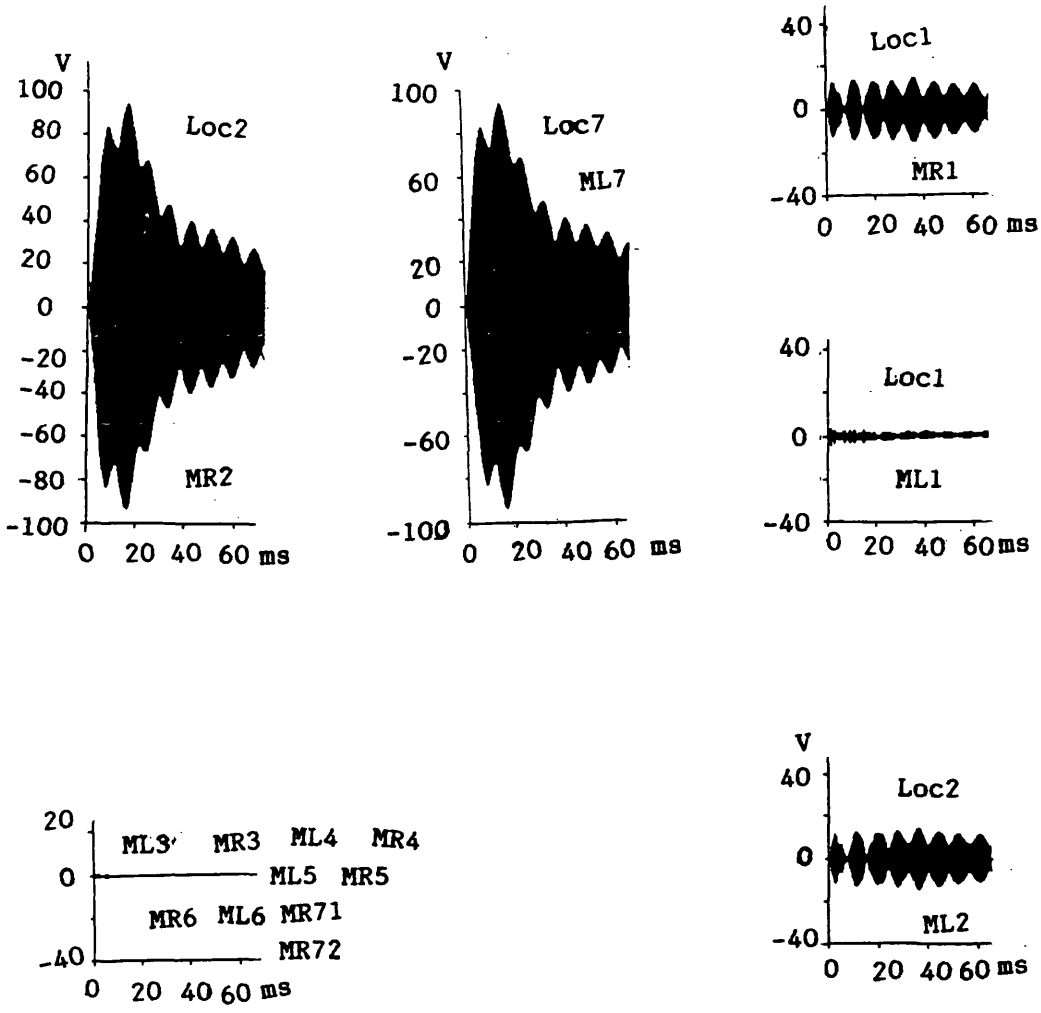


Figure 12.10a
Modal output signal voltages from fault locator after lightning stroke hiting on the 11kV system with capacitor banks

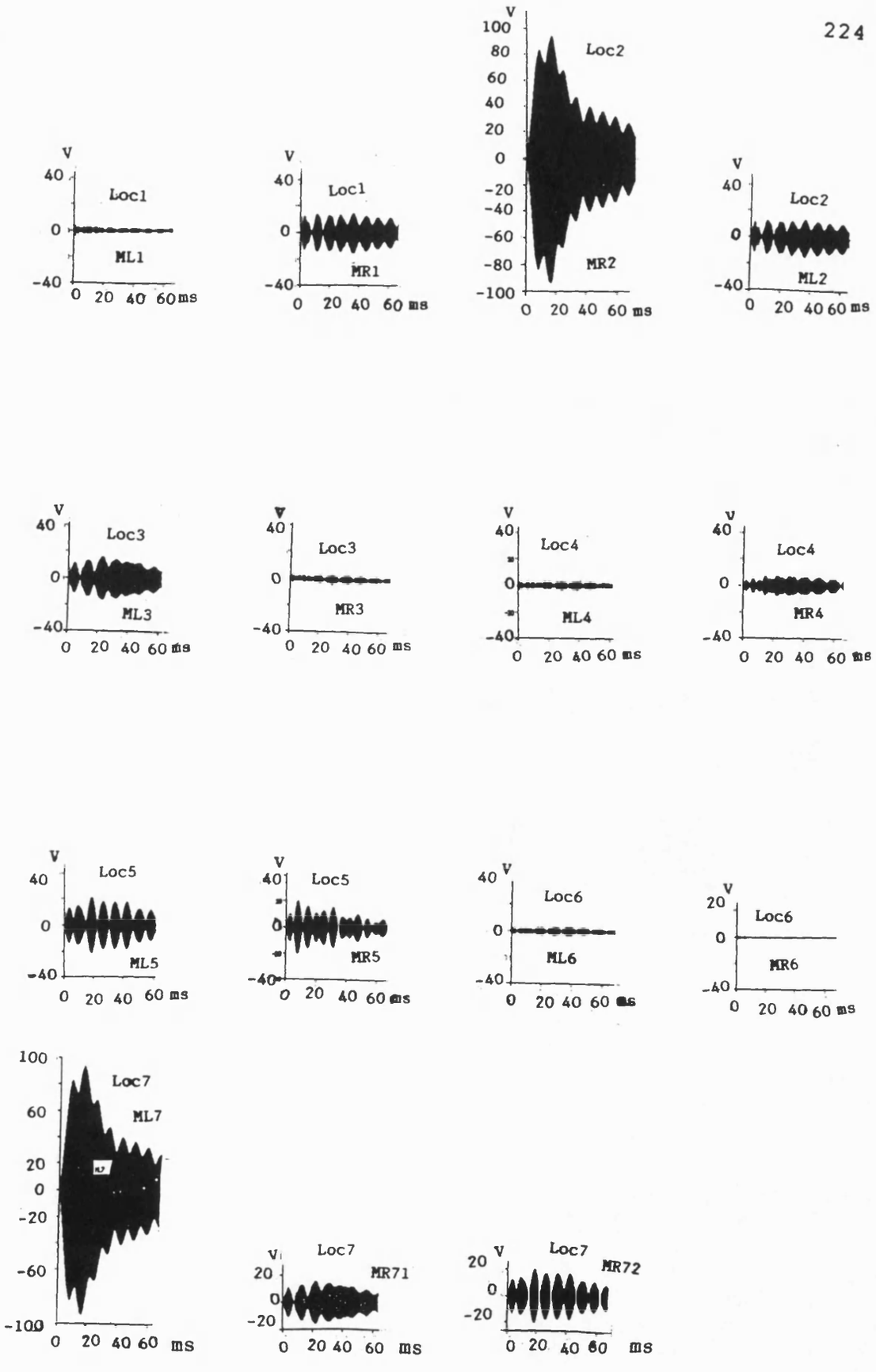


Figure 12.10b
Modal output signal voltages from fault locator after lightning stroke hiting on the 11kV system without capacitor banks

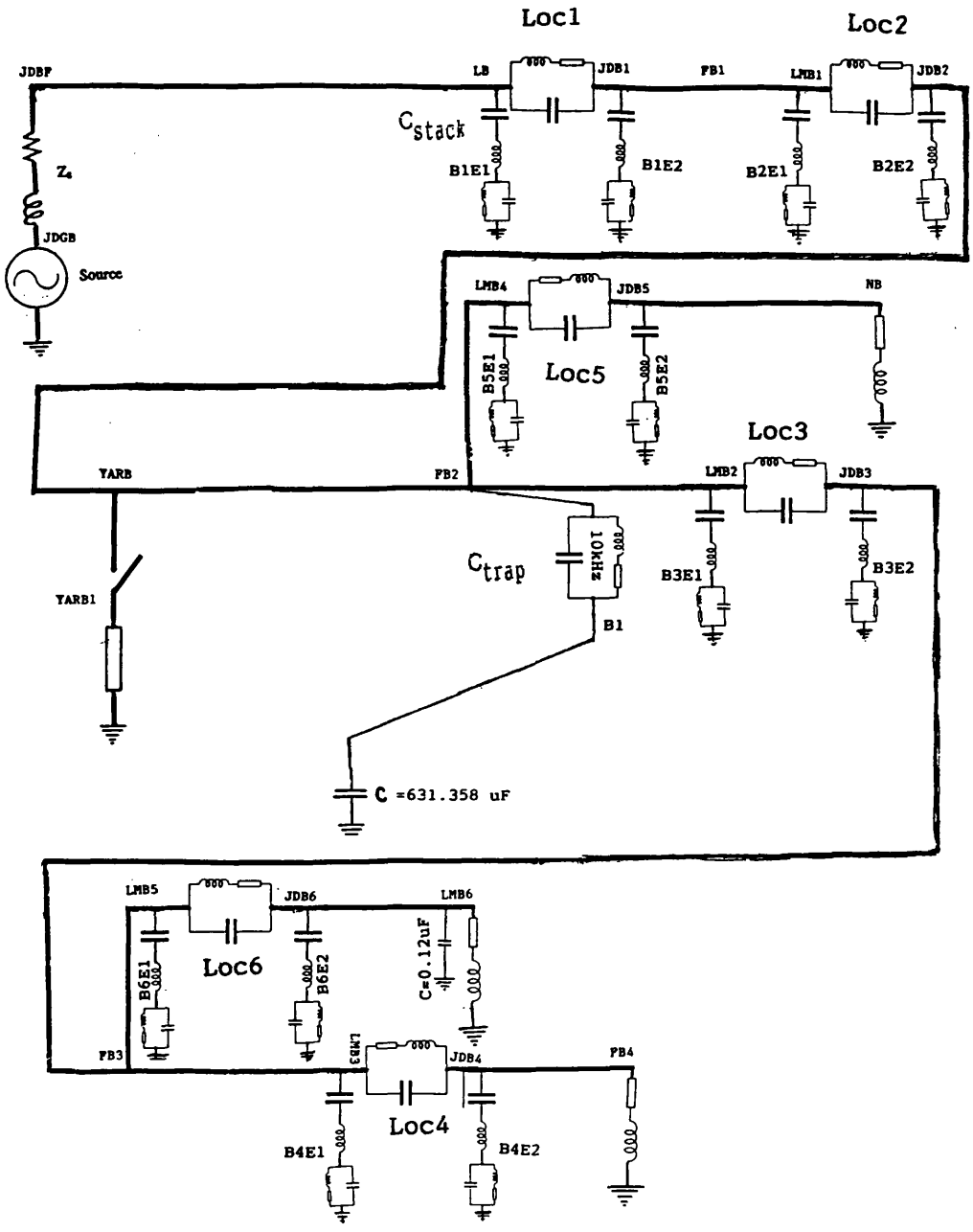
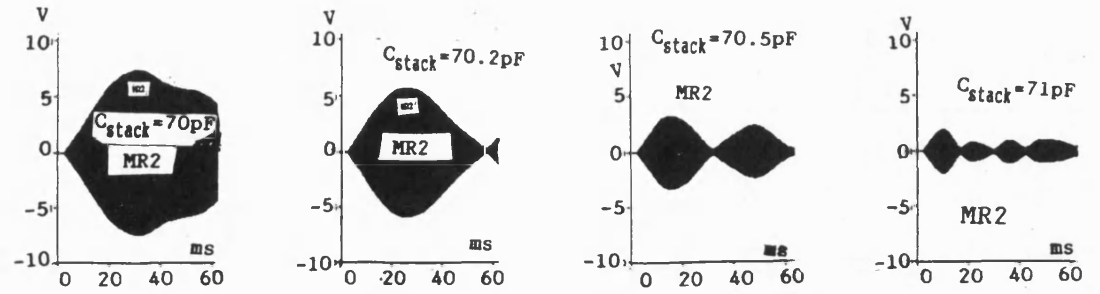
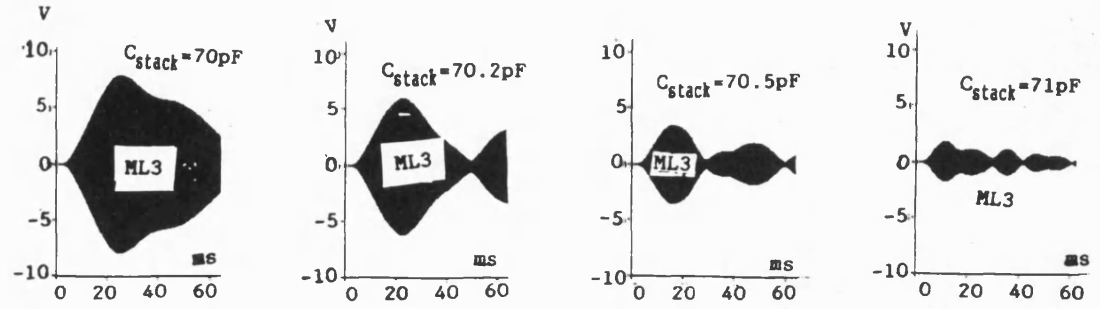


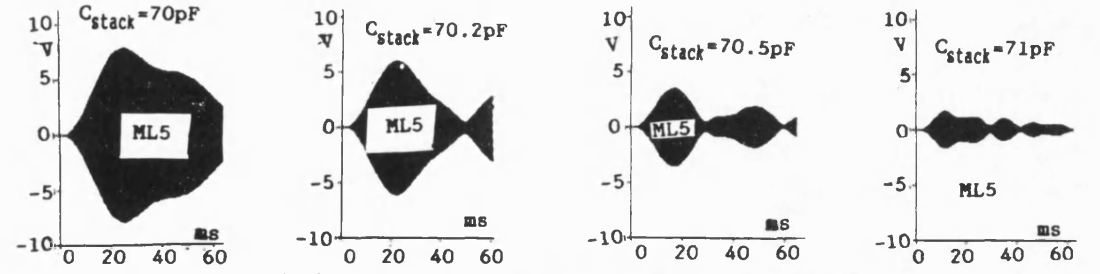
Figure 13.1
Circuit arrangement for sensitivity analysis for the effect of a marginal change in the parameters of the fault locator



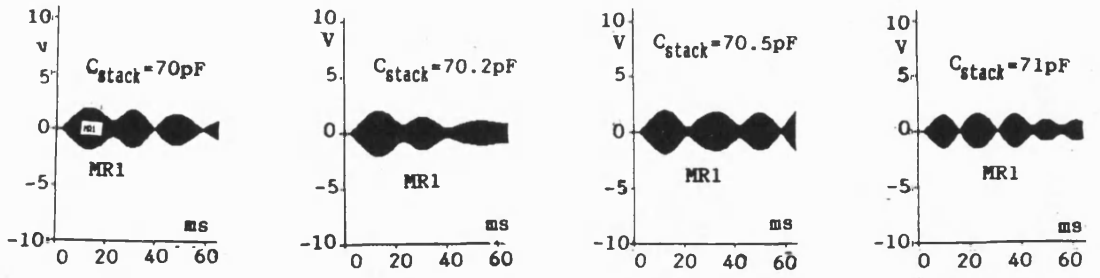
(a) signal output MR2 from Loc2



(b) signal output ML3 from Loc3



(c) signal output ML5 from Loc5



(d) signal output from fault locators (MR1) away from fault

Figure 13.3
Comparison of fault locator outputs for 4 different values of C_{stack}

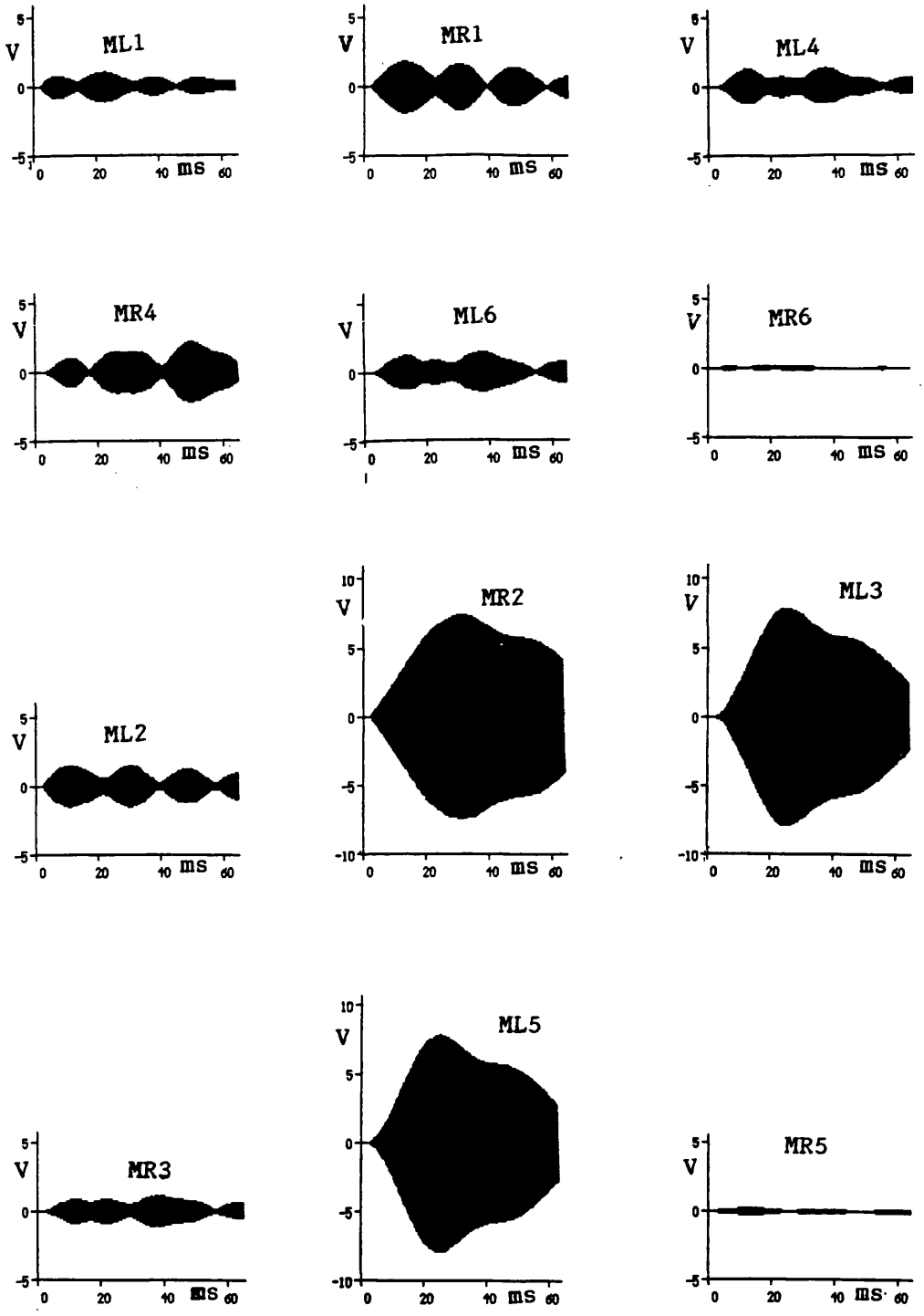


Figure 13.2
Fault locator signal outputs in modal form at designed parameters

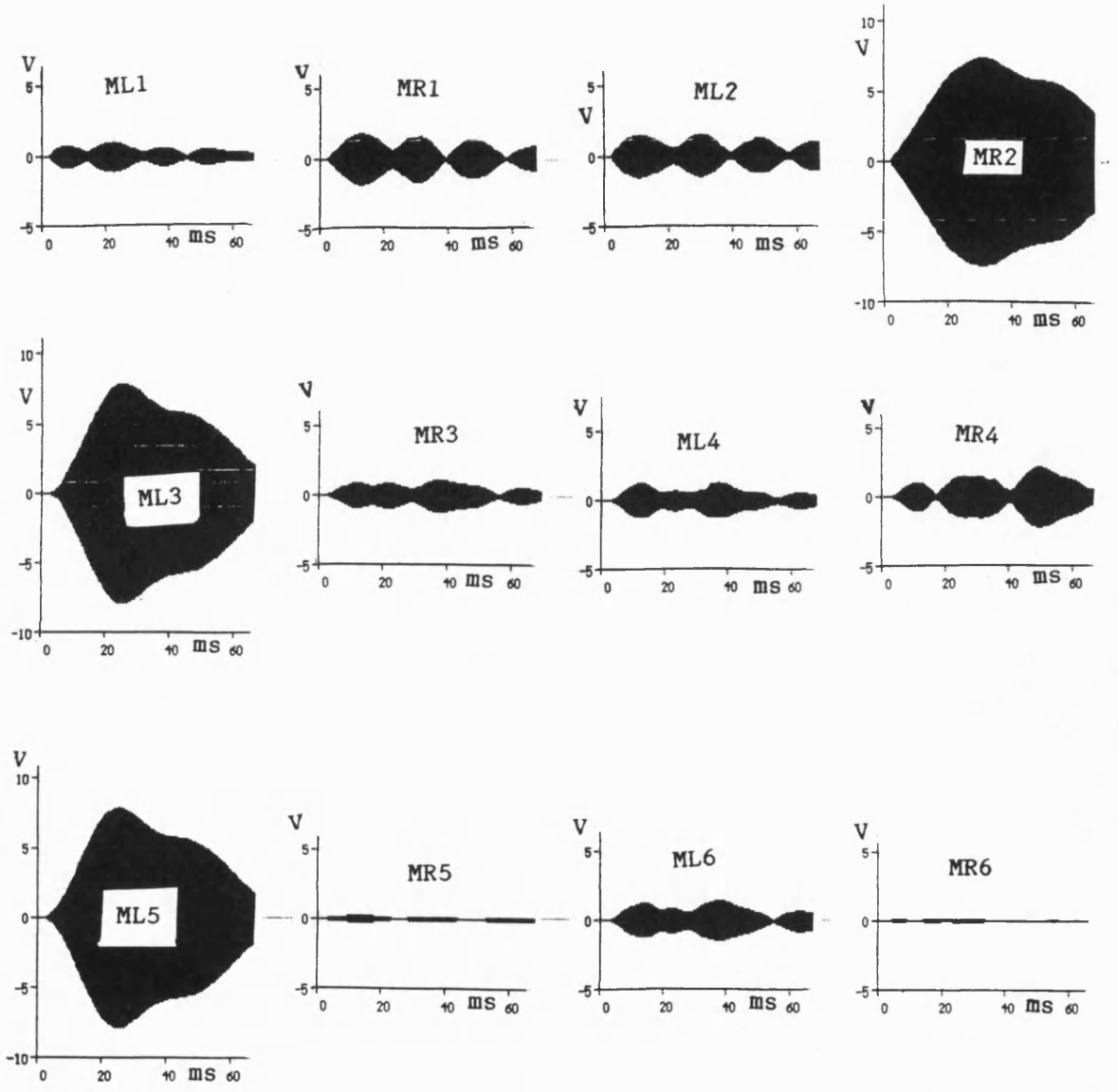


Figure 14.1
Performance of the fault locator at f_0=10kHz

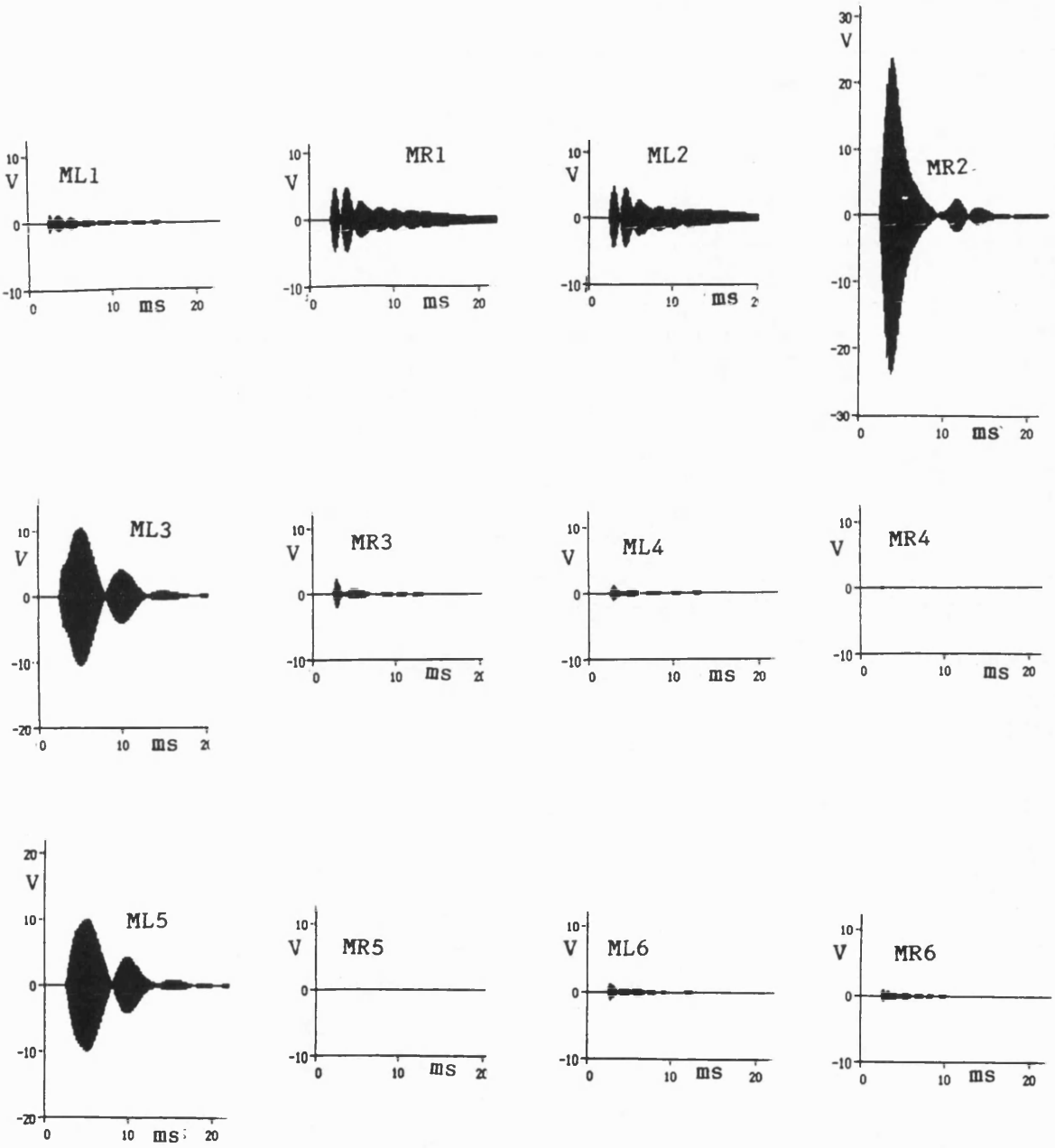


Figure 14.2
Performance of the fault locator at f_0=50kHz

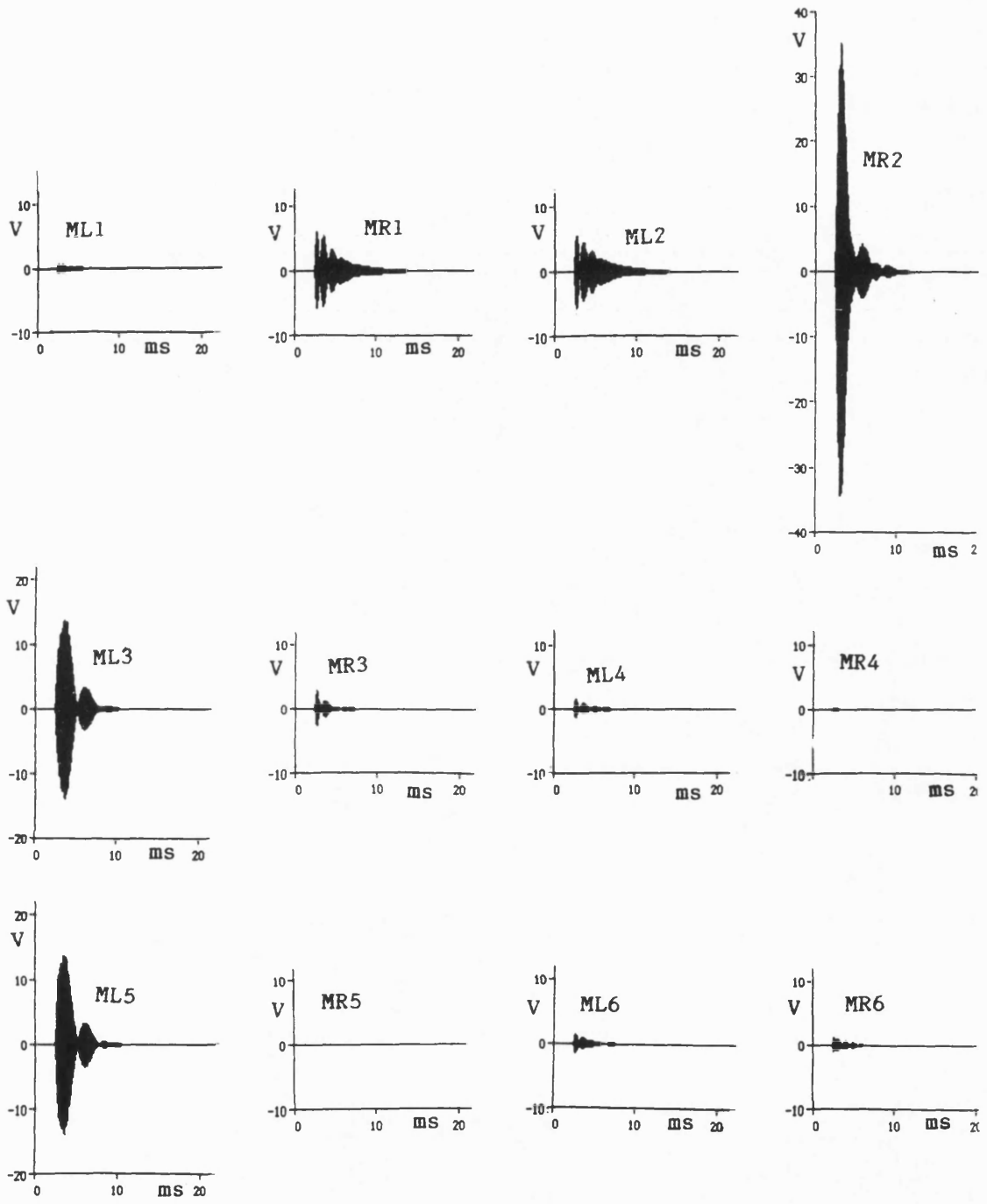
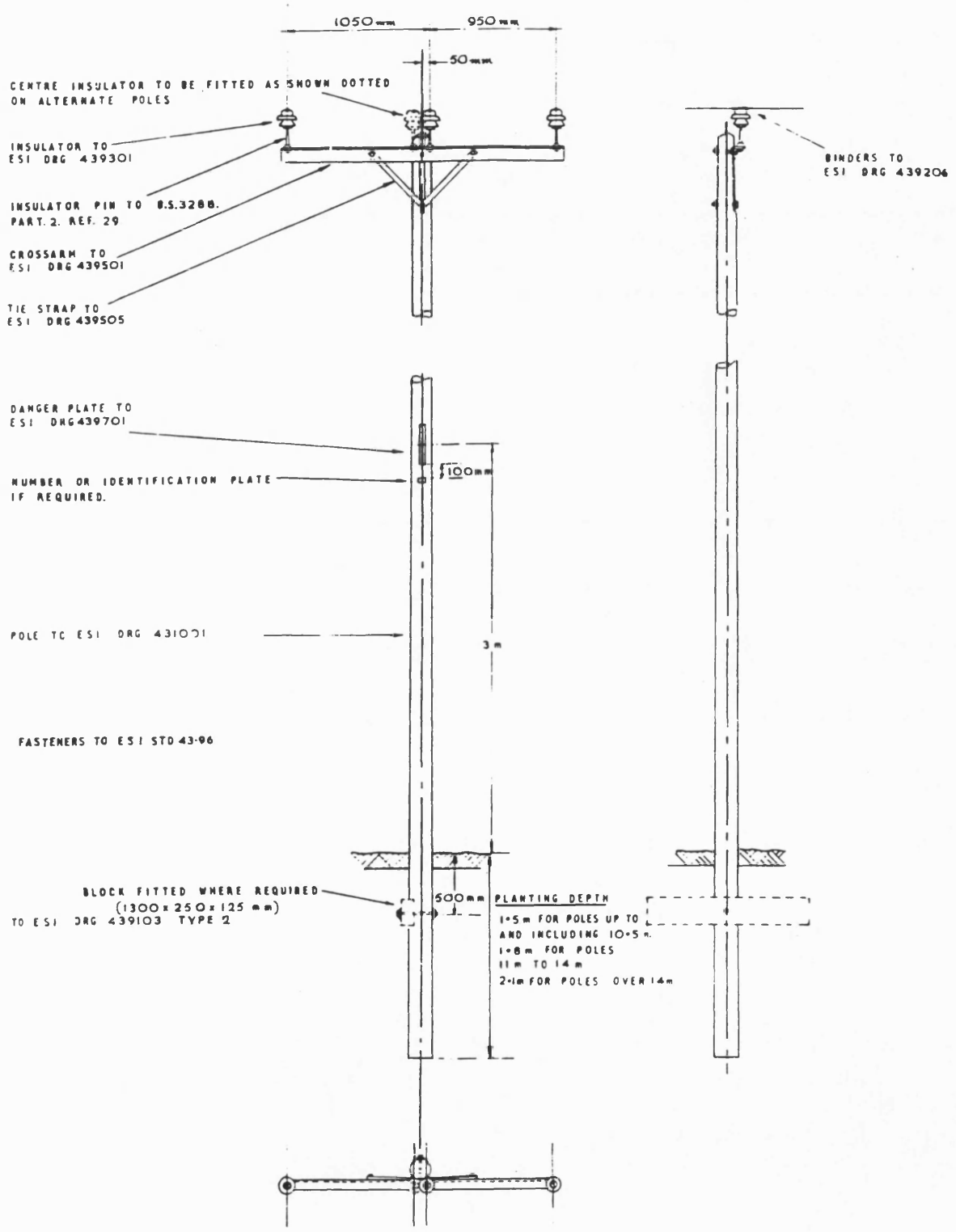


Figure 14.3
Performance of the fault locator at f_0= 90kHz



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General assembly – intermediate pole

WEB 43-93/2
Issue 2
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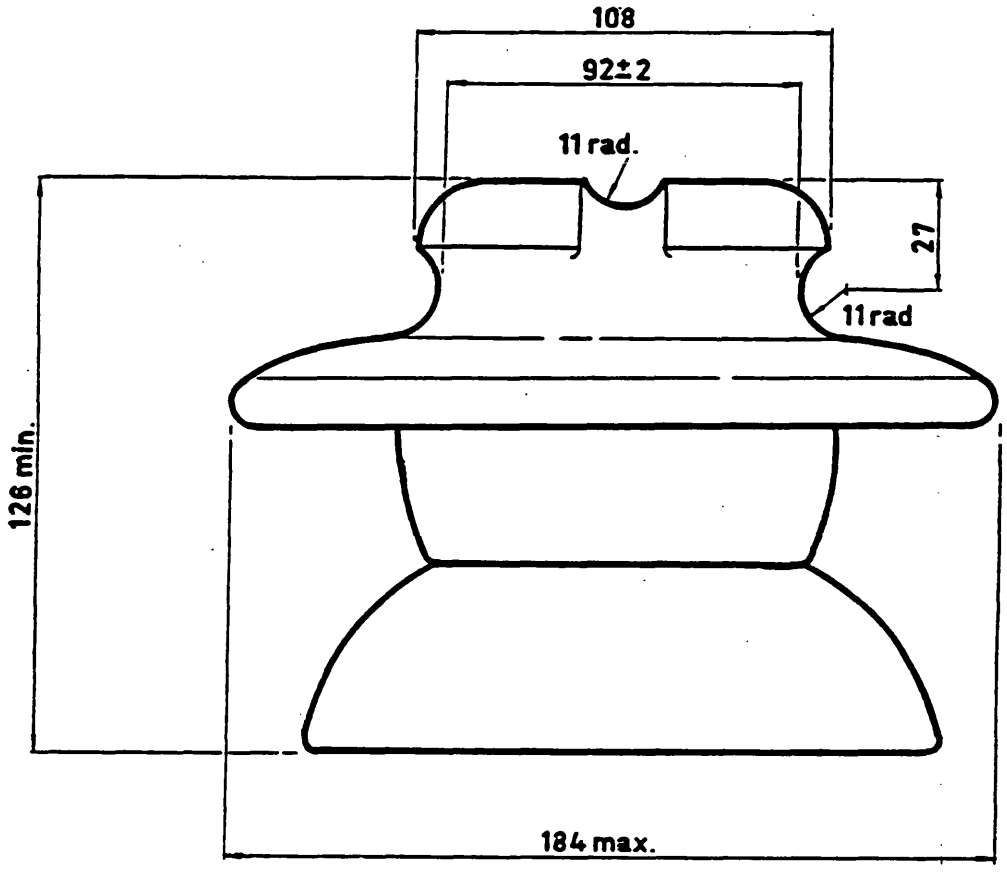
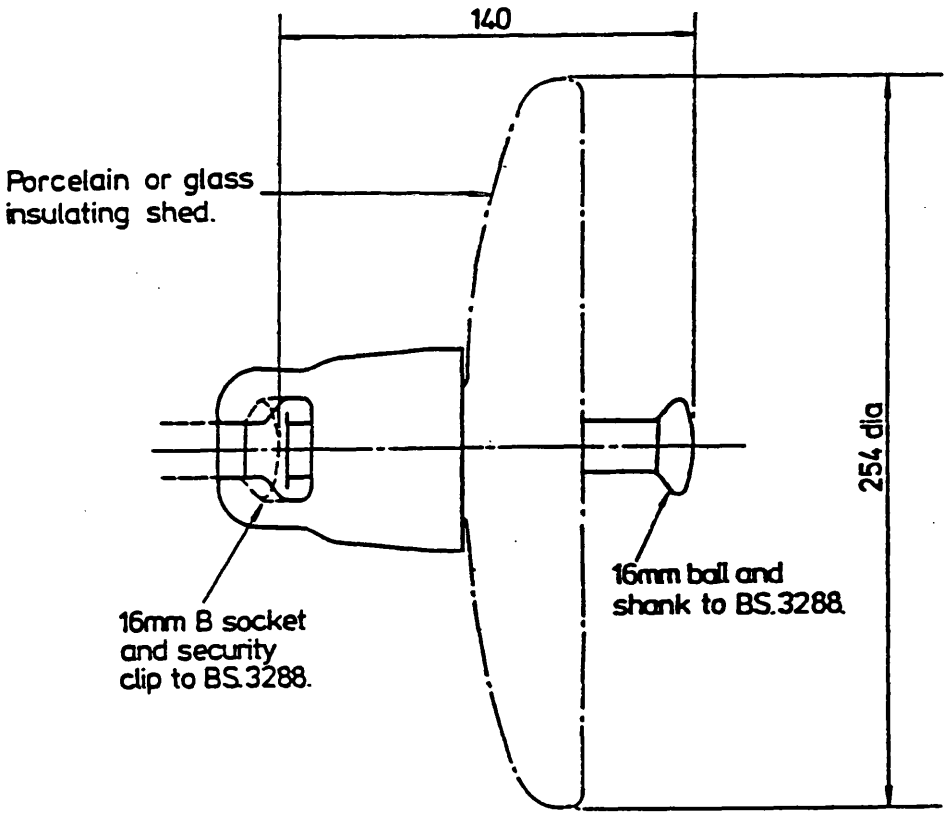


NOTES

1 In accordance with BS 137
2 Total creepage distance 324 min
3 Dimensions in millimetres

INSULATOR–11kV PIN TYPE
(For exceptional pollution conditions)



Note:

1 All dimensions in millimetres.

2 Insulator in accordance with BS 137 and as illustrated on ESI Drawing 439306.

TYPICAL STRING INSULATOR UNIT

11kV OVERHEAD LINES COPPER AND ALUMINIUM ALLOY CONDUCTORS

CONDUCTOR SPACING A 1.0 m B 1.2 m

	COPPER CONDUCTORS					AL. ALLOY CONDUCTORS				
	A	A	B	B	B	A	A	B	B	B
1. Designated Size Nominal Cross Section Sq.mm.	16	32	25	70	100	25	40	50	100	150
2. Stranding No./Diam. mms	3/2.65	3/3.75	7/2.14	7/3.55	7/4.30	7/2.34	7/2.95	7/3.30	7/4.65	19/3.48
3. Effective cross sectional area sq.mms	16.44	32.93	25.02	68.80	100.9	29.78	47.33	59.22	117.6	177.9
4. Diameter overall mms.	5.69	8.05	6.42	10.65	12.90	7.02	8.85	9.90	13.95	17.40
5. Weight of one conductor Kgs per Km	148.3	296.9	255.7	621.0	911.2	82.0	131	164	325	497
6. Resistance D.C. ohms per Km at 20°C	1.0830	0.5410	0.7114	0.2585	0.1763	1.0940	0.6880	0.5498	0.2769	0.1830
7. Resistance A.C. ohms per Km at 20°C	1.0830	0.5412	0.7114	0.2588	0.1768	1.0940	0.6880	0.5500	0.2772	0.1834
8. Reactance Ohms per Km	0.4064	0.3846	0.3882	0.3753	0.3629	0.3884	0.3734	0.3775	0.3554	0.3418
9. Impedance Ohms per Km	1.1567	0.6639	0.8104	0.4560	0.4037	1.1609	0.7828	0.6671	0.4507	0.3879
10. % R on 100 MVA Base per Km	89.50	44.73	58.79	21.39	14.61	90.41	56.86	45.45	22.91	15.15
11. % X on 100 MVA Base per Km	33.59	31.79	32.08	31.02	29.99	32.10	30.86	31.20	29.37	28.25
12. % Z on 100 MVA Base per Km	95.60	54.87	66.97	37.69	33.36	95.94	64.69	55.13	37.25	32.06
13. Charging current amps per Km per phase	0.018	0.019	0.018	0.020	0.020	0.019	0.020	0.019	0.021	0.022

LTS 10/72
Revised 11/85

O/H Line Constants
11kV Metric Copper and Silmalec
D3 M. 3.1

Positive Sequence Impedance	R_1 ohms/km	1·083	0·541	0·711	0·259	0·177	1·094	0·688	0·550	0·277	0·183
	X_1 ohms/km	0·405	0·383	0·407	0·375	0·363	0·390	0·376	0·380	0·358	0·342
Zero Sequence Impedance	R_0 ohms/km	1·231	0·689	0·860	0·407	0·325	1·242	0·836	0·698	0·495	0·332
	X_0 ohms/km	1·753	1·732	1·721	1·689	1·677	1·738	1·724	1·694	1·672	1·656

Subject Area: 2 235

DISTURBANCES AND PROTECTION IN SUPPLY SYSTEMS

12th International Conference on ELECTRICITY DISTRIBUTION

Part 1: Contributions

IEE Conference Publication No: 373

DESIGN PROGRESS OF A NEW DISTRIBUTION SYSTEM FAULT LOCATOR

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University Of Bath, U.K.

1. Introduction

The design progress of the fault locator which is described in previous papers [1,2] is reported in this paper. However it is found that to enhance the performance of the fault locator further investigation had to be carried out to achieve practical parameters for the fault locator elements. The paper reports the reasons for the changes with the new corresponding parameters and performance.

2. Description of the new fault locator[1]

The studies in ref.(1) proved the viability of the fault locator with one trap circuit surrounded by the shunt stack tuner circuits from which the up and down stream signals are obtained. The latter two signals are refined and fed to a directional decision circuit by which the direction of the fault is determined. With a distributed number of fault locators the exact location can then be obtained.

To explain the principle, the original form of the fault locator was designed[1] on the principle of a single trap circuit which is comprised of three parallel tunable circuits to resonate at the same tuning frequency of the stack tuner of 100 kHz.

Now to develop an immune circuit against radio frequency interference, it is found that operational frequency of 10 KHz is practical. Furthermore for faults occurring at near voltage zero crossing, the probability of a reliable measurands is found at the lower frequencies around 10 kHz.

On the other hand the old design produces a narrow operating band and therefore a wider operating frequency band is required. When further studies of the trap tuner were carried out and especially when taking into consideration the frequency dependent of the trap tuner reactor, the frequency band required better attention.

Widening the operating frequency margin enables better performance and the studies showed that twin trap tuner circuits connected in series is sufficient. The tuning frequencies of those tuners are chosen within ± 50 Hz from the 10 kHz which the shunt stack tuners are tuned.

Fig 1 shows the circuit diagram of the new stack tuner fault locator. The inclusion of the self resistance of the reactor within the tuner branch should be noted. The parameters at 10 kHz are;

L1 = L2 = 0.1 mH R1 = R2 = 0.0001 ohms

C1 = 2.5368 µF C2 = 2.5298 µF

C = 70 pF L = 3.618 H

R_o = 400 ohms K = 14.5

3. Comparative performance of the old and new designs

Fig 2 shows a comparison between the old single trap and the new twin trap circuit measured impedances. As can be seen at 4 k.ohms the bandwidth is widened from 12 to 32 Hz. Furthermore Fig 3 shows that while the minimum ratio of the output to input voltages has gone down from 0.05[1] to 0.0296, now the operating margin at 0.05 is widened to 20 Hz.

4. An overview on the power system simulation

To examine the fault locator, an accurate power system simulation is required. It is evident that the majority of faults will be of the earth type faults. This requires proper simulation of arcing faults.

Arcs in power systems can be found in various types. Some of these are resulting from shunt true faults but others can develop from series healthy faults such as those arising from circuit breakers opening or closing. A similar series arc would be blowing a fuse in a distribution circuit.

While frequency dependent parameters of the distribution lines and associated fault locators can nowadays be simulated in a Fourier domain of analysis, arcs possess a nonlinear time domain characteristic of the form given in fig. 4. The latter shows that the voltage across the arc is current dependent and when it is linearised for computer applications fig 5 shows the approximate cyclogram of the voltage current dependent arc utilised.

Another aspect of arcs are those developing from partial discharges prior complete breakdown of insulations which could be found within transformers or across porcelain insulators of overhead lines. Such problems are characterised by a beating phenomena and can also be detected or restrained. The phenomena is described in ref.6 for further information.

Generally, it should be noted that the high frequencies superimposed on the fault voltages are partly due to the arcs and partly due to switchings on non homogeneous lines e.g. a fault occurring on a multi-tapped line. Numerous computer trials for different system configurations are being examined to assess the selected tuning frequencies of the fault locator.

Details of the arc simulation can be found in references 3,4 and 5.

5. Simulation Results

Figs 6 and 7 show the superimposed filtered voltages of the up and down streams stack tuners. Fig 8 shows typical energy levels of fault locators distributed on the same feeder which by careful selection of the threshold level the fault can be located.

6. Other design aspects

The schematic diagram of the fault locator is given in fig 9. Also the prototype being developed is shown in fig 10 where it should be noted that the tuner reactor will have a centre tap (not shown in the photograph) to provide access to the twin trap tuners. The cross section of the reactor is chosen to withstand 100 MVA short circuit level with a proper cooling arrangement to withstand 5000 amps for 1 sec and for a continuous withstand of 50 amps according to BS5253:1975 for 12 KV rated voltage. This is to facilitate direct insertion of the fault locater within the distribution systems and avoiding extra costs which could result in utilising current transformers.

The feasibility of remote fault locating is also being studied so that, with different tuning frequencies for different fault locators, the fault location can be estimated by scanning the remaining frequencies at the primary substation. The studies will be reported soon as the size of this paper does not allow expanding to these studies.

Field tests are being planned which will be reported in due time.

7. Acknowledgement

The preliminary works by Mr Daruvala D., Dr. El-Hami M.and Dr. Li L. are appreciated. Some of these works are reported in this paper as the present works are a continuation of the same research facilities provided by the British Technology Group (BTG), London, which is also highly appreciated. Finally thanks are due to the University of Bath for permission to publish the paper.

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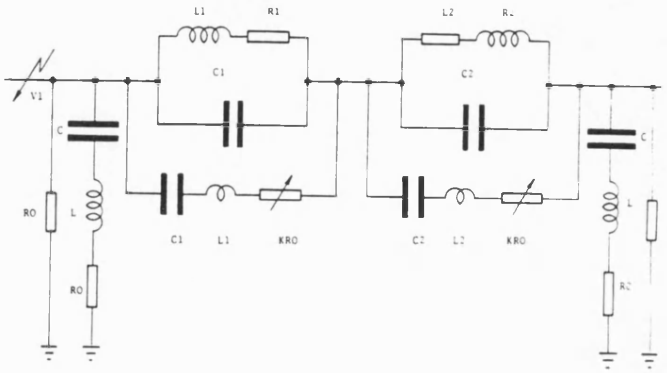

Fig 1 Circuit diagram of the Stack Tuner

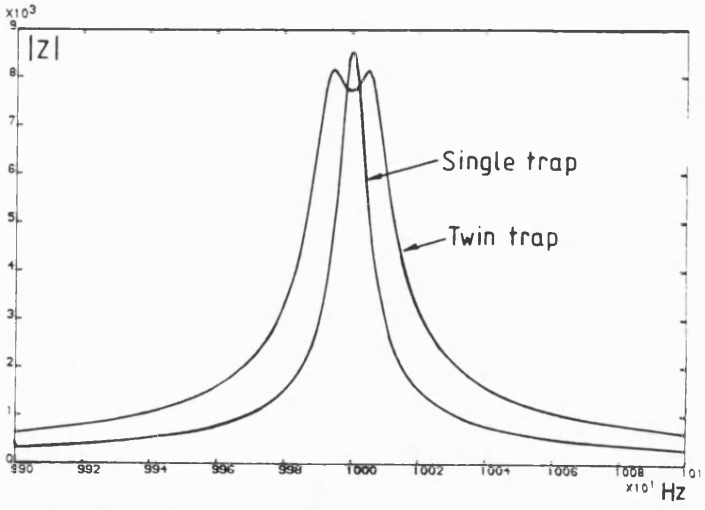

Fig 2 Comparison between the circuit impedances of the single and twin trap tuners

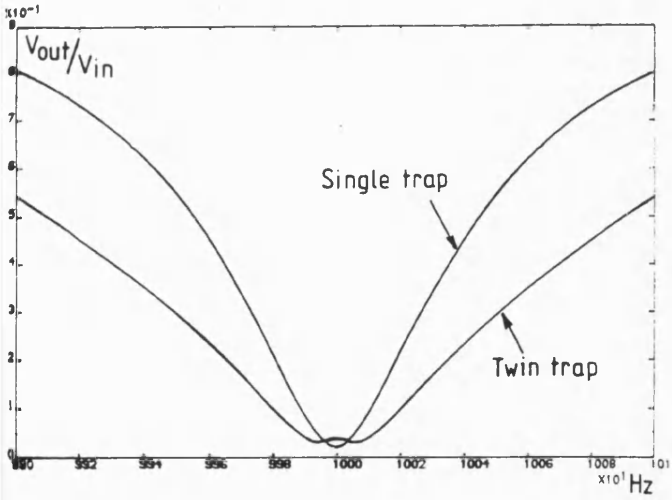

Fig 3 Output to input voltage ratio of the stack tuner

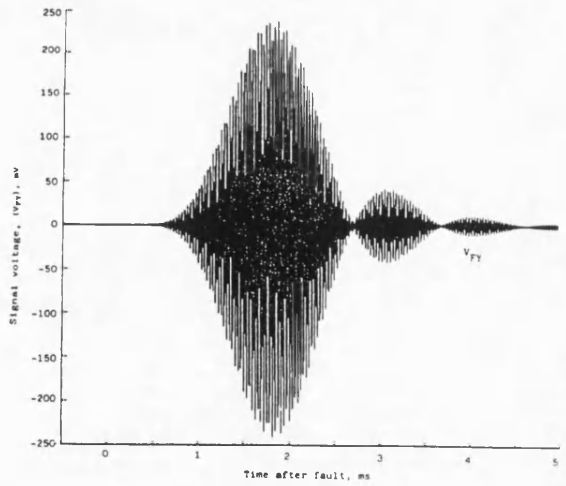

Fig 6 Down stream superimposed fault voltage signal

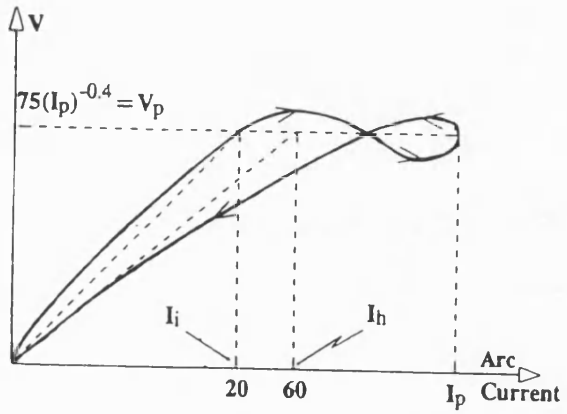

Fig 4 Typical arc cyclogram for the voltage current dependent arc

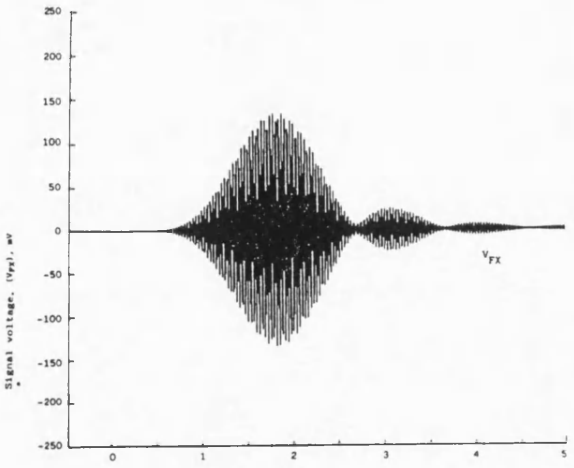

Fig 7 Up stream superimposed fault voltage signal

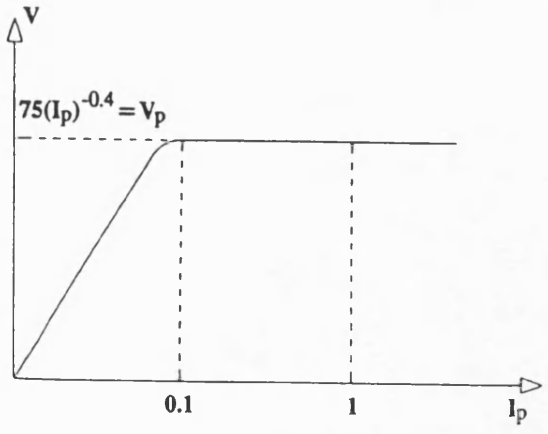

Fig 5 Piecewise linear approximation of the arc cyclogram shown in fig 4

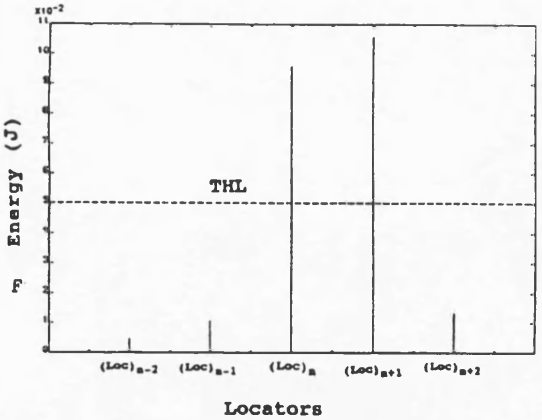

Fig 8 Typical energy levels of fault locators distributed on the same feeder

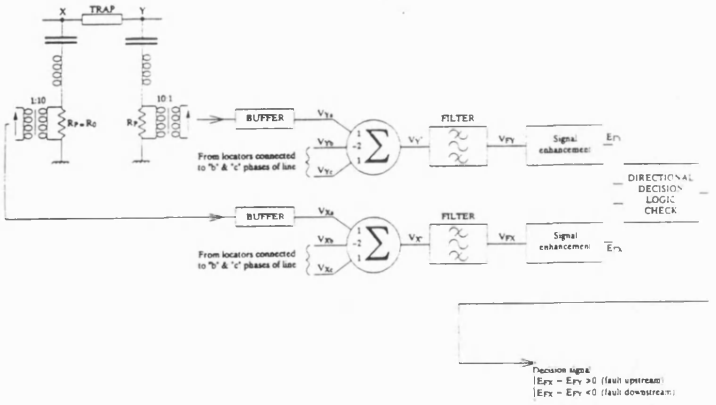

Fig 9 The schematic diagram of the fault locator

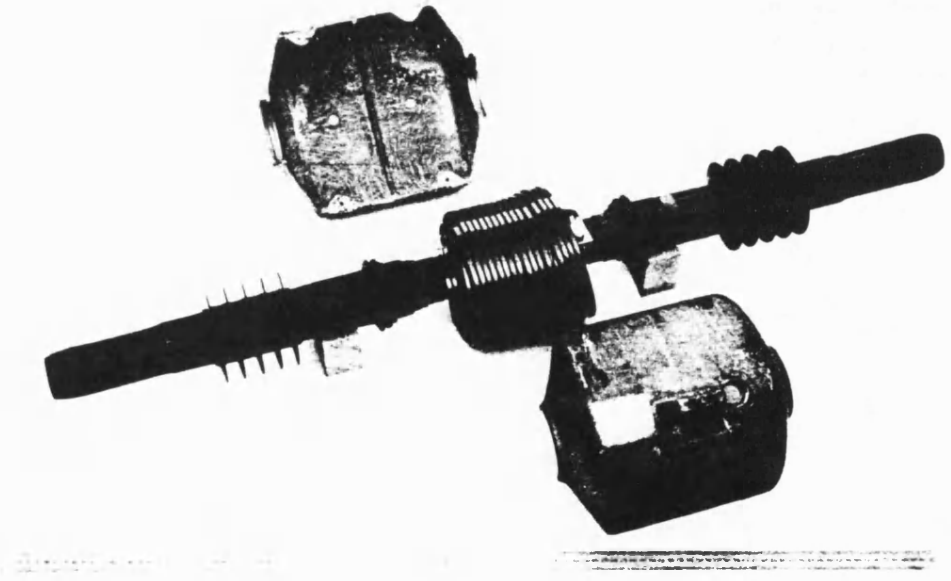

Fig 10 The prototype of the fault locator being developed by the Power & Energy Group The University of Bath, England

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DEVELOPMENTS IN THE DESIGN OF A FAULT LOCATOR FOR DISTRIBUTION SYSTEMS

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1. INTRODUCTION

This paper reports the further development that is taking place following the work progress given in ref.(1). While the final design of the fault locator is not ready this paper investigates the possible design and performance when analogue filtres are refined and used within the primary part of the fault locator to lessen the use of digital components of the secondary part.

Ref.(1) described the design progress of the fault locator taking advantage of previously accepted digital filtering technique(2). The modification made in the fault locator, resulted in a better performance compared to the originally introduced in ref.(2) as it widened the bandwidth of operation but at a new middle frequency of 10 kHz. This is in contrary to the narrow bandwidth and the 100 kHz of the original design(2) which was mainly to explain the principle of the use of fault noise for fault locators. That previous(2) design proved to produce unreliable outputs. To achieve higher output and faster response, it became necessary to improve filtration.

The performance of the latest fault locator is presented in this paper and the conclusion is hence drawn.

2. FUNCTION OF THE NEW FAULT LOCATOR

Fig.(1) shows the previous fault locator(1), which has an LCR wide band pass filter in stack tuners S1 and S2 together with a narrow parallel LCR band reject filter in the trap tuning circuit T1 and T2. With a fault at point F, fault noise frequencies travelling at both directions along the power line, away from F, is produced. The trap circuits T1 and T2 stop a narrow band of particular frequencies B with a centre frequency wo rad/s (10kHz). These narrow band frequencies are now available in the output of the stack tuners S2 and S3 which are nearest to F. As a result of the attenuation taking place in the tuners T1 and T2, these narrow band frequencies are suppressed at the output of the stack tuners S1 and S4.

All the stack tuners possess wide bandpass series LCR filtres of the same characteristic, same cutoff frequencies and same bandpass frequencies (mB) centred around the same centre frequency of T1, where m lies between 10 and 20 as explained in ref.(3). The outputs of S2 and S3 differ to the outputs of S1 and S4 only by the presence of the frequencies within the bandwidth 'B' in S2 and S3. As the range of 'B' frequencies is a small part compared to mB frequencies, the outputs of all alike stack tuners possess the same shape, ie same shape for the mB's and similarly for the B's stacks.

It may now be said that the fault location, where series LCR stack tuners are applied, is not secure unless the outputs are filtered externally either by digital or analogue filtering. For this reason alone the previous fault locators(1,2) were totally dependent upon the external filtration.

Now consider new design in fig.(2), it has the same trap circuit as in fig.(1) but differs in the stack tuner. The trap circuits T1 and T2 stops same frequencies B (centred around wo). The series LCR stack tuners are now replaced by a reduced bandpass parallel circuit stack having a bandpass width of (1/2)B centred around wo.

In a similar fashion S2 and S3 to the previous locator will output the B/2 frequencies which will not exist in S1 and S4. This technique securely locates the fault by the directly available signals.

3. EFFECT OF PARAMETERS ON FILTRATION

The stack tuner of this latest fault locator consists of two filters connected in series, each filter working on same resonant frequencies wo.

The purpose of first LC series filter is to provide very high impedance at low power frequency (50 Hz) and to cancel the effect of capacitor C at resonant frequency wo such that the combined effect of L and C provides a zero impedance at wo.

The second filter is a parallel resonant circuit. The parallel esonant circuit depends upon L4,C4 and R4 parameters. The parallel resonant circuit fulfils four purposes, (i) provides an impedance (equal to surge impedance of power lines) at wo and surrounding frequencies, (ii) provides zero impedance for all remaining frequencies, (iii) creates output voltage across both ends of the impedance only during wo and surrounding frequencies, (iv) provides output voltage across the terminals at both ends of the parallel circuit. These operations of the parallel circuit makes it a perfect filter circuit for fault locators. These characteristics help the stack tuner to act as a filter circuit for output across parallel branches. At resonant frequency wo, the output is very high and at off the resonant frequencies the output is low and theoretically zero.

For a constant value of wo, if L4 is changed, the corresponding values of R4 and C4 also change. Using computers to obtain the effect of each set of L4, C4 and R4 values upon the frequency bandwidth, it is found that increase in the value of L4, widens the bandwidth of the parallel resonant circuit and vice versa. From the same computer program,

42

it is further observed that an increase in the value of R4, increases the bandwidth of the filter frequencies but decreases the total impedance of the parallel resonant circuit at wo. However, an increase in bandwidth due to an increase in R4 can be compensated by a decrease in the value of L4. Thus by adjusting L4 and R4, both requirement specifications (i) the bandwidth of filter frequencies and (ii) the total impedance of the parallel resonant circuit at wo, are controlled.

The combined operation of both the series and parallel filters, working at same resonant frequency wo, as shown in below, provides a single filter having characteristics of both filters. Thus this stack tuner circuit has high total impedance at around power frequencies, but an impedance equal to surge impedance of power lines at wo and surrounding frequencies. This is beside the narrow band filtration and filtering only for the specified frequencies.

4. FORMATION OF EQUATIONS

From the circuit impedance shown in fig.(2), the following relationship is obtainable;

$$L = \frac{1}{C\ wo^2} \qquad (1)$$

Similarly for very small value of R4, C4 is obtained as in equn.(2)

$$C4 = \frac{1}{L4\ wo^2} \qquad (2)$$

Now the impedance of parallel filter is equal to surge impedance Ro of the power lines at wo for which it can be shown that;

$$R4 = L4/(C4.Ro) \qquad (3)$$

5. DESIGN PROCEDURE FOR THE STACK TUNER

The design of the stack tuner now depends upon the following information ard equations (i) The centre operating frequency wo (ie fo) of the fault locator. (ii) The value of C which depends upon physical structure of the trap circuit and dielectric between the trap circuit and the supporting electric lines etc. (iii) The prestated design equations 1 to 3. (iv) The calculation of L4 is obtained from the following relationship;

$$L4 = n.(k/D).L1 \qquad ----------(4)$$

where n=1,2,3....N shows nth calculation of L4. Also k/D is a constant. k and D are arbitrary parameters to fix the initial value of L4 and to smooth the difference between two adjacent values of L4. For instance for L1 = 0.1 mH, then k/D = 6/1000.

Based upon these values, the frequency response of Fig.(3), for n=1,2,... is drawn. Curve for n=5 shows B/2 bandwidth frequency characteristics for design of the new stack tuner.

6. RESULTS and DISCUSSION

Fig.(4) shows an analogue output from the stack tuners S2 and S3 closest to F, see fig.(2), whereas figure 5 shows an analogue output from the far end stack tuners S1 and S4. On comparison of fig.(4) to fig.(5), it shows that the output magnitude (energy) of the signal in fig.(4) is much higher than the output from the far off stack tuner signal in fig.(5). The two outputs are clearly different and much easy to discriminate.

With careful handling of the outputs from the stack tuners adjacent to the fault is enough to operate an electronic, or logic relay. This result confirms that the fault locator is properly functioning and that the fault location is securely achieved by the new design changes and that the new fault locator does not require external analogue or digital filtration.

7. ACKNOWLEDGEMENTS

Mr. Burdi is indebted to the British Council and ODA for the full financial support to do PhD at Bath University.

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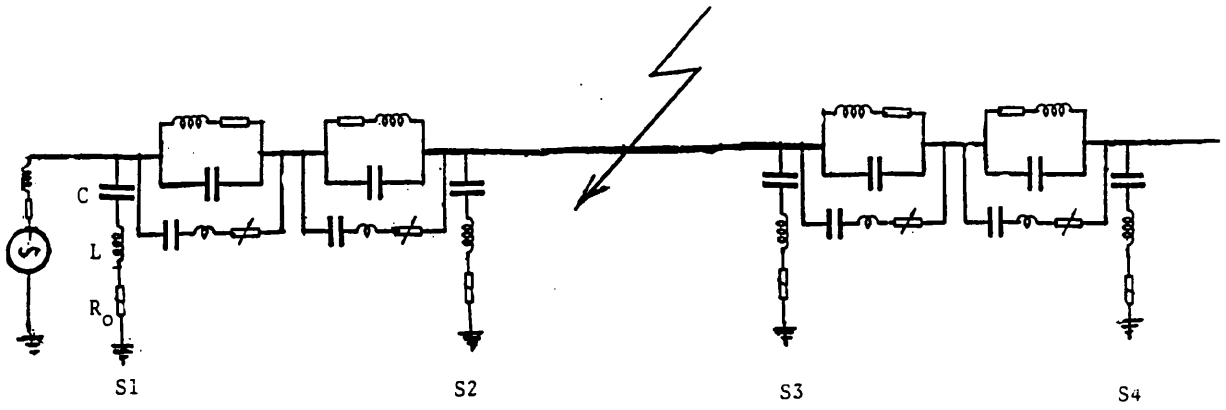

Fig.1 The previous Fault locator using Series CLR resonant circuit for the stack tuner.

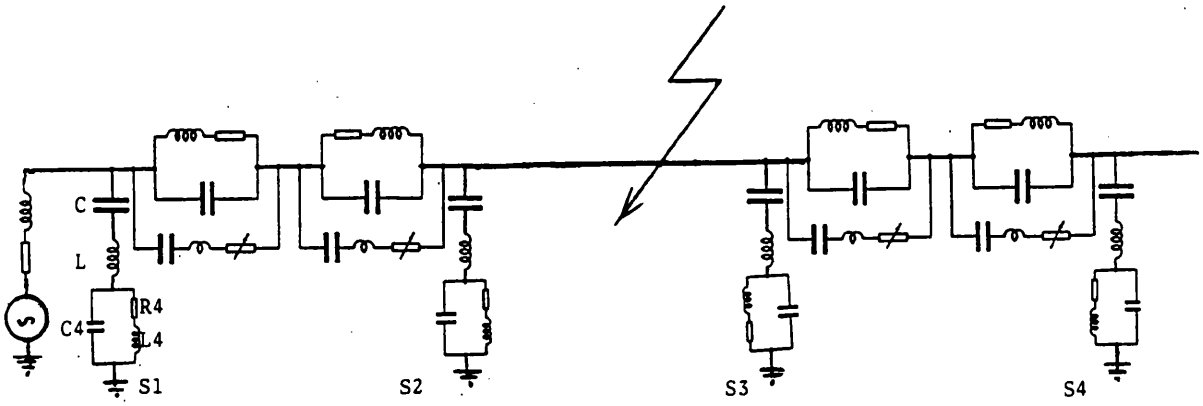

Fig. 2 The new fault locator combining (i) Series LC resonant circuit and
(ii)a parallel RLC resonant circuit for the Stack Tuner

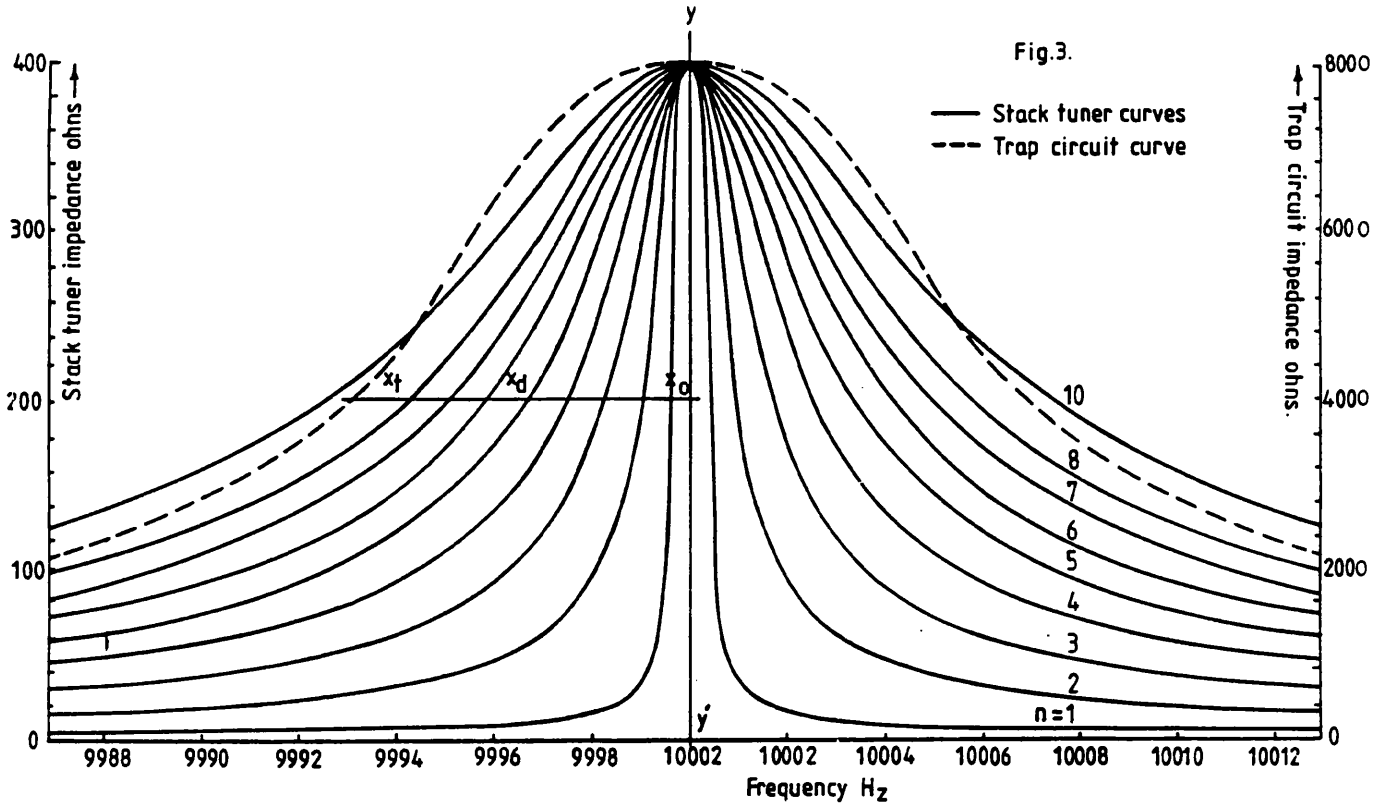

Fig. 3 Impedance versus frequency for the stack and trap tuner for accurate Bandwidth design

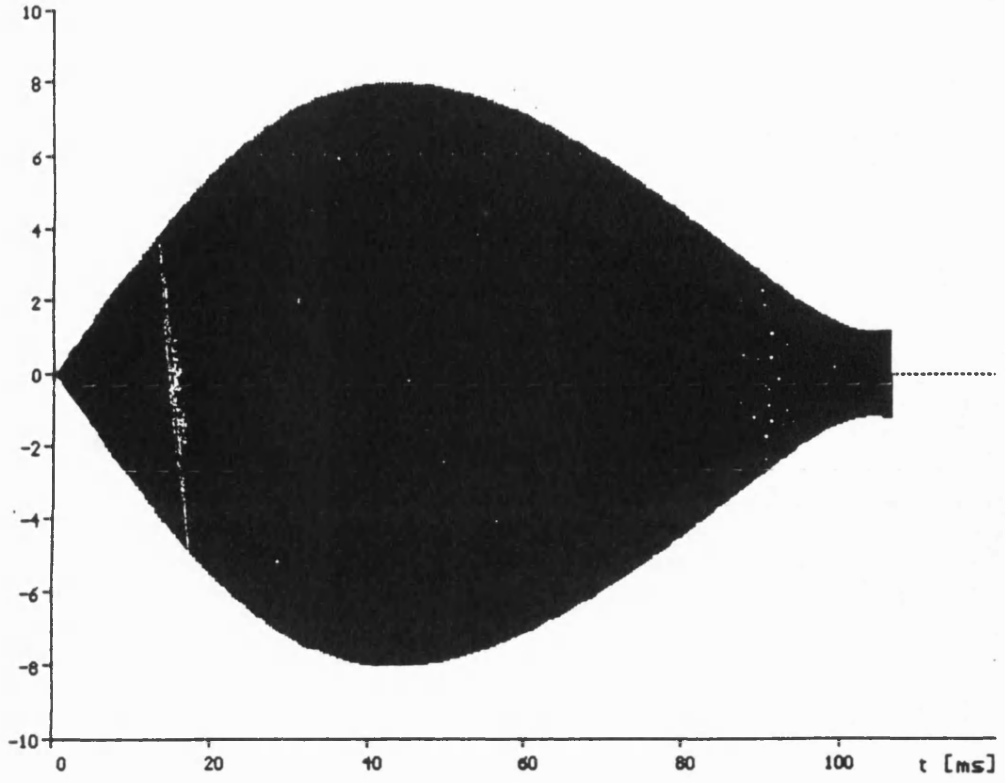

Fig. 4 Output from Stack Tuners outputs S_2 and S_3, the closest to the fault point F

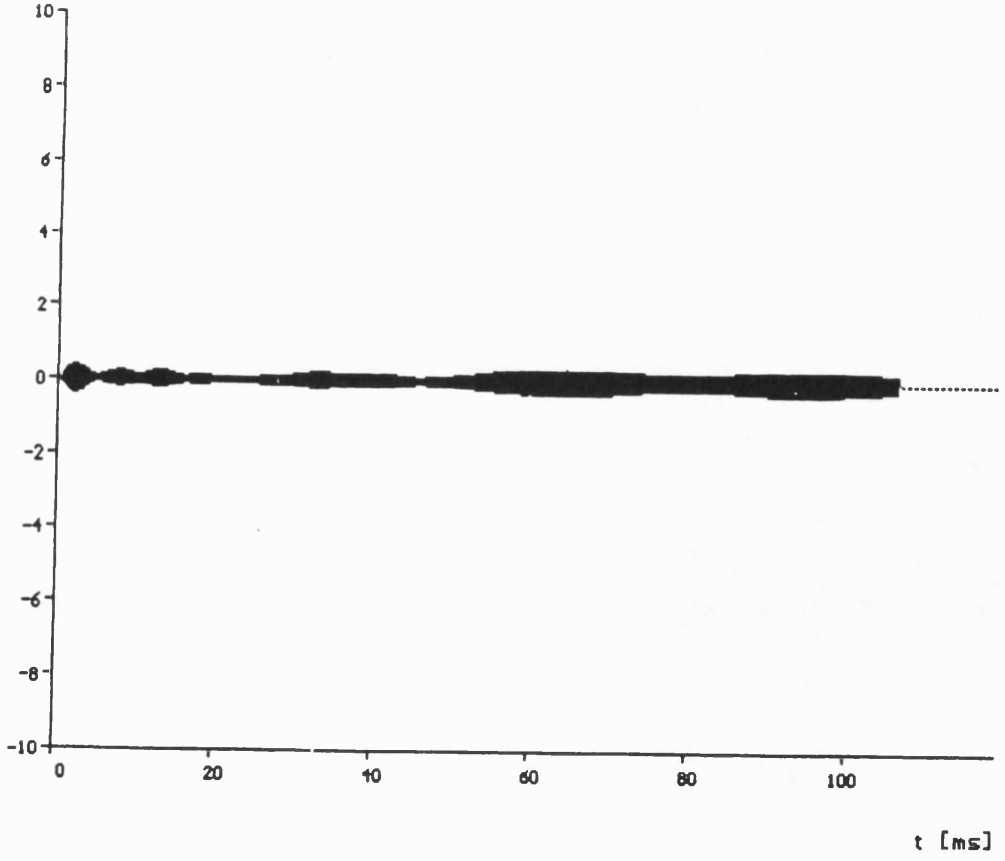

Fig. 5 Output from Stack Tuners S_1 and S_4, far from the fault point F.